Low-Voltage, High-Brightness Silicon Micro-LEDs for CMOS Photonics

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(Invited Paper)

***Abstract*— Silicon photonics realized in CMOS processes has transformed computing, communications, sensing, and imaging. Although silicon is an indirect bandgap material prohibiting efficient light generation, considerable work has been conducted in the field of silicon p-n junctions emitting broadband visible light when operating in the high-voltage reverse breakdown avalanching mode. Here, we demonstrate high-brightness near-infrared (NIR) light emission for forward-biased silicon micro-light emitting diodes (micro-LEDs) realized in an open-foundry microelectronic CMOS process—55 BCDLite—with zero modification. Under room-temperature continuous-wave operation, the external light emission intensity of over 40 mW/cm^2 at a central wavelength of 1020 nm is achieved for a 4-μm-diameter device at below 2.5 V. This is realized by adopting a deep vertical junction with guard ring designs that ensure carrier transport away from the device surface and material interfaces where nonradiative recombination usually dominates. Here, we also demonstrate a complete chip-to-chip communication link using only standard multimode fiber and monolithically integrated CMOS micro-LEDs and detectors.**

***Index Terms*— CMOS, light emitting diode (LED), micro-LED, optical communication, silicon photonics.**

I. Introduction

ELECTRONIC and photonic technologies have transformed our lives—from computing and mobile devices to information technology and the Internet of Things. Our future demands in these fields require innovations in each technology separately but also depend on our ability to harness their complementary physics through integrated solutions. Silicon CMOS has been adapted to realize optical functions ranging from waveguiding and photodetection to optical filtering and modulation. However, the indirect bandgap of silicon has severely limited the availability of CMOS light sources suitable for communication and sensing applications.

Light emission intensity and efficiency from semiconductor materials are the results of competition between different carrier recombination processes. Assuming that both the electron and hole concentration in a device active region are $n(=p)$, the spontaneous emission rate in the Boltzmann limit can be described by $R_{sp} = Bn^2$ with a bimolecular recombination coefficient B, which is material-specific. The primary competing nonradiative recombination processes include surface recombination at material boundaries and interfaces, the bulk Shockley–Read–Hall (SRH) recombination via defect states, and the Auger recombination. Their corresponding nonradiative recombination rates are described by $S_{\text{eff}} n A_a / V_a$, where S_{eff} is surface recombination velocity (SRV) of a specific material interface and A_a/V_a is the ratio of the active region area to volume, An, where A is the bulk-SRH coefficient, and Cn^3, where C is the Auger coefficient (for the sum of electron capture and hole capture processes), respectively. The carrier density-dependent radiative recombination efficiency, or the internal quantum efficiency η_{IQE}, can, thus, be defined as

$$\eta_{\text{IQE}} = \frac{Bn^2}{S_{\text{eff}} \frac{A_a}{V_a} n + An + Bn^2 + Cn^3}. \tag{1}$$

Radiative recombination in silicon is phonon-assisted, which results in a bimolecular recombination coefficient that is many orders of magnitude smaller than those in direct-bandgap materials, as summarized and compared in Table I [1]–[6]. However, the potentially high quality of bulk silicon material and effective surface passivation indicated by the nonradiative coefficients are also much smaller. In 2001, Green *et al.* [7] demonstrated silicon electroluminescence with peak external quantum efficiency (EQE) as high as 0.55% in a macroscopic 20 mm × 20 mm vertical solar cell with passivated surfaces and dedicated extraction structures biased at only 0.7 V. This remarkable conversion efficiency for an indirect-bandgap semiconductor was achieved at a relatively low light intensity of 0.3 mW/cm^2. Furthermore, (1) suggests that, as devices scale to smaller sizes, nonradiative surface recombination becomes dominant for all materials. For micron-scale devices, effective passivation (and, thus, very low SRV) of silicon [1]

TABLE I
Comparison of Recombination Coefficients (300 K)

Material	SRV S_{eff} ($cm\ s^{-1}$)	Bulk-SRH A (s^{-1})	Radiative B ($cm^3 s^{-1}$)	Auger C ($cm^6 s^{-1}$)
Si [1-3]	$10^{-1} - 10^{1}$	$10^{4} - 10^{5}$	4.7×10^{-15}	3.8×10^{-31}
GaN [4]	10^{4}	$10^{7} - 10^{8}$	2.0×10^{-11}	2.0×10^{-30}
GaAs [4-6]	10^{6}	$10^{7} - 10^{8}$	1.7×10^{-10}	7.0×10^{-30}
InP [4-6]	10^{5}	$10^{7} - 10^{8}$	2.0×10^{-11}	9.1×10^{-30}

Manuscript received April 5, 2021; revised May 19, 2021; accepted May 25, 2021. Date of publication June 14, 2021; date of current version July 23, 2021. This work was supported in part by the Agency for Science, Technology and Research (A*STAR), Singapore, and in part by the Kwanjeong Educational Foundation. This article is an extended version of a paper presented at IEDM 2020. The review of this article was arranged by Editor T. Grasser. *(Corresponding author: J. Xue.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3085541.

Digital Object Identifier 10.1109/TED.2021.3085541

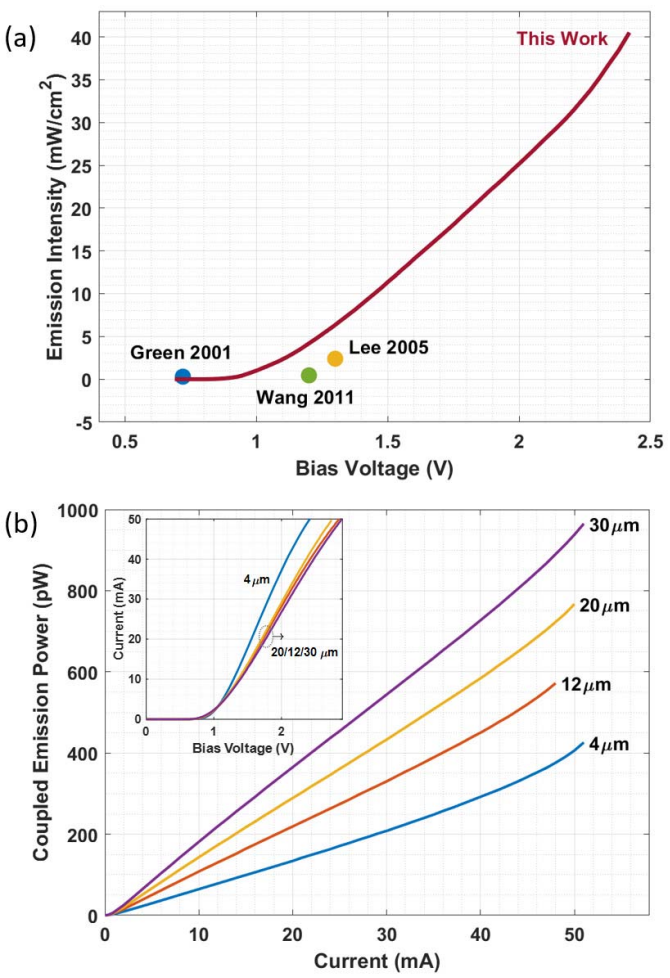

Fig. 1. (a) External emission intensity versus forward voltage for a 4-μm diameter CMOS LED developed here. A few data points from the literature are shown as well for comparison. (b) *L–I* curves for CMOS LEDs of the same (optimal) design but with various active device diameters. Emission is butt-coupled to a standard 50-μm-core multimode fiber for power measurement. Inset shows the corresponding *I–V* curves.

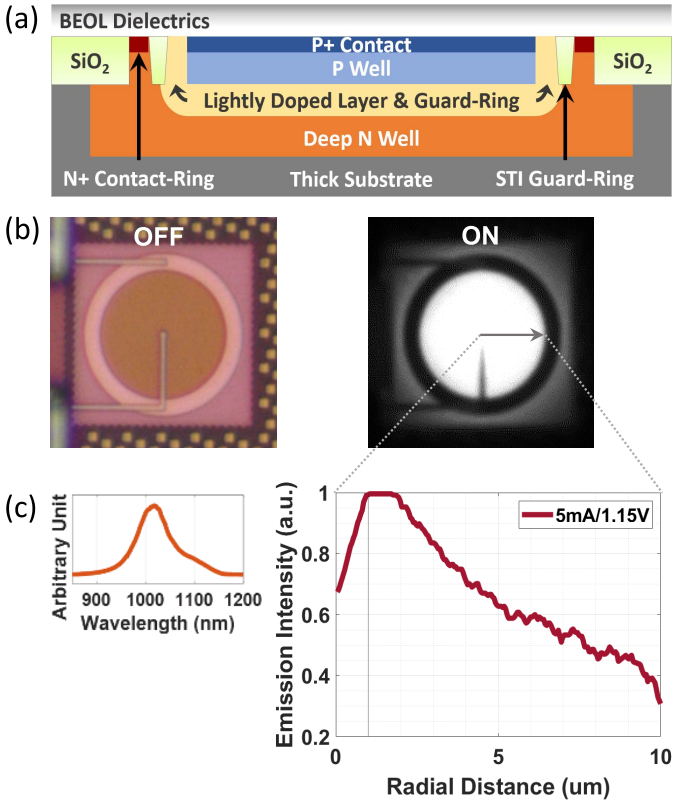

Fig. 2. (a) Schematic junction structure (optimal) for the CMOS micro-LED developed here. (b) Micrograph of a 20-μm-diameter CMOS LED and its NIR light emission operating at 10-mA forward current viewed with a CMOS camera with 30-s integration time. (c) Emission profile of radial intensity distribution for the device operating at 5 mA with inset on the left showing its emission spectrum. Intensity drop near the center is due to light blocking by metal contact.

should result in relatively low total nonradiative recombination rates.

There have been a few examples of submillimeter silicon light emitting diodes (LEDs) in CMOS technologies, for example, [8]–[11], which exploits hot carrier electroluminescence associated with reverse-biased avalanche multiplication [8], [9] or bimolecular recombination in forward-biased diodes [10], [11]. Avalanche-mode LEDs (AMLEDs) provide broadband optical emission partially overlapping the visible spectrum but have very low internal quantum efficiency and relatively high reverse voltages (5–17 V). Several attempts to reproduce the performance of Green's forward-biased, low-voltage silicon LEDs in CMOS technologies have yielded low-intensity light emission as well [10], [11], as shown in Fig. 1(a). All these previous demonstrations of nonavalanche mode light emission from silicon CMOS have focused on lateral diode junction structures.

Here, we report on vertical-junction silicon micro-LEDs with significantly higher brightness in low-voltage forward-bias operation at room temperature. These devices are demonstrated in an unmodified, open-foundry microelectronic CMOS node, which is a variant of bipolar-CMOS–DMOS (known as BCDLite) scaled to 55 nm. Compared to the previously reported lateral-junction designs, the vertical junction: 1) supports operation at higher current bias without efficiency droop and 2) allows radiative recombination to take place away from the silicon surfaces where nonradiative recombination would be greater. We also scale the device dimension down to 4 μm, which is comparable to the smallest mesa size of state-of-the-art III-Nitride-based micro-LEDs [12]. The high brightness of the CMOS micro-LEDs allows us to couple light directly into standard multimode fiber typical of data communications. The coupled light can be detected by an integrated CMOS avalanche detector realized in the same technology.

II. Device Description

A. LED Device Structure

Previously reported CMOS LEDs operating in both forward and reverse bias most often adopted lateral junctions near the silicon top surface. In this work, a circular CMOS device is designed with a lightly doped vertical junction formed between a P-well and a deep N-well at just over one micron deep, as shown in the doping profile illustrated in Fig. 2(a). This vertical junction serves as the active region of the device, and light is emitted through the entire top surface (through BEOL dielectrics). The deep N-well here is typically used for improved substrate noise isolation in triple-well MOSFET devices and for electrical isolation of

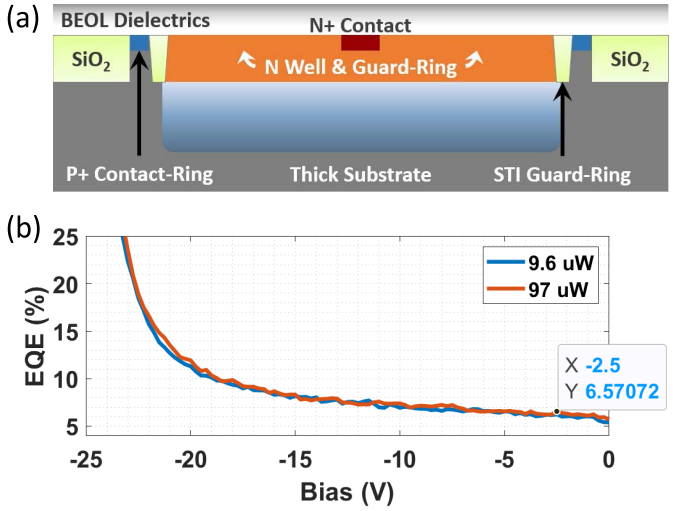

Fig. 3. (a) Schematic junction structure for the CMOS photodetector developed here. (b) EQE under $\lambda = 1$-μm illumination of two different incident power levels for a photodetector of 20-μm diameter.

high-voltage DMOS devices. P+ and N+ implants are applied at selected areas of the device, respectively, to form the anode and cathode contacts. A guard ring is incorporated, including a lightly p-doped silicon region (inner) and shallow trench isolation (STI) of oxide (outer). The lightly doped region can be realized with an implant block layer typically used for resistive guard rings that reduce substrate noise coupling. A small-area metal contact (so as to minimally block the light emission) is used to inject current into the top central P+ region. As shown in Fig. 2(b), devices are implemented in the 55-nm BCDLite process with no modification or custom layer. No postprocessing or packaging is made.

In order to illustrate the benefits of the optimal design choice described above, we have also designed and measured several variants of it considering: 1) shallow junctions; 2) n-p and p-n vertical junctions; and 3) exclusion and modification of the lightly p-doped guard-ring region next to the STI. The performance of these variants illustrates the importance of junction design and guard ring optimization.

B. Photodetector

A Geiger-mode photodetector of 20-μm diameter designed in the same process is used to collect the LED light emission. As shown in Fig. 3(a), we found that a detector using the p-substrate as part of the p-n junction achieves good detection. The device EQE under $\lambda = 1$-μm illumination of two different incident power levels is shown, respectively, in the figure, indicating an over 6.5% efficiency at -2.5-V reverse bias even for a wavelength in the near-infrared (NIR) regime. This device has a breakdown voltage of -24.2 V and can be operated in the Geiger mode to achieve efficient detection at low light levels. At a moderate over the bias of 0.9 V, the measured dark count rate (DCR) is approximately 1 kcps (3.2 Hz/μm^2).

III. Device Characterization

A. I–V Curve

Fig. 1(b) presents the I–V curves for the CMOS micro-LEDs in the inset. Devices with a diameter ranging from 4 to 30 μm were evaluated. The devices exhibit consistent turn-on voltages in the room-temperature forward-bias operation. The smallest diameter device exhibits the lowest parasitic series resistance and also achieves the highest current density—both are an indication that the spreading resistance is an important contribution to the parasitic series resistance.

B. Optical Emission Characterization

The optical emission from these devices is characterized using three different methods: 1) microscopic imaging of the light emission using a cooled CMOS camera; 2) measurement of the emission spectra using a 50-μm-core multimode fiber coupled to a spectrometer; and 3) measurement of the fiber-coupled or free-space collected optical power using an InGaAs power meter.

A micrograph of NIR emission from the top surface through BEOL of a 20-μm-diameter CMOS LED operating at 10-mA forward current is shown on the right-hand side of Fig. 2(b). This image is taken by a cooled CMOS camera with a 50x objective (NA = 0.55) in the dark for 30-s integration time. While the entire area of the LED appears bright under high injection, a quantitative analysis for the radial intensity distribution at a lower injection current of 5 mA reveals that the light emission intensity is brightest near the center of the device (but away from the central contact) and diminishes at the outer edges by approximately 60%, as indicated in Fig. 2(c). The emission is observed to be bright until the boundary of the STI guard ring.

The light emission from the device's top surface can then be directly butt-coupled to a standard multimode optical fiber of 50-μm-core diameter for spectroscopy measurement. A cleaved fiber tip is aligned to the top of the device with an air gap of a few micrometers in-between to avoid contact and damage. No focusing or collimating optics is used. The left-hand side of Fig. 2(c) shows the measured optical spectrum using an IR-enhanced deep-depletion silicon CCD, indicating band-to-band emission.

The total optical power coupled into the optical fiber is measured using an optical power meter with a calibrated InGaAs detector. Fig. 1(b) shows the coupled emission power as a function of bias current for devices of different diameters. As expected, the larger area devices emit more output power—with the 30-μm devices emitting 0.95 nW into the multimode optical fiber at a 50-mA injection current. The efficiency of fiber coupling from the LED is less than 8%. This bound is determined by comparing the fiber-coupled optical power of a 4-μm device to direct free-space collection using a microscope objective of high collection efficiency (NA = 0.95 and magnification: 50×) and correcting for its spectral transmission. The highest external emission intensity is observed for the smallest device (4-μm diameter), achieving 40.6 mW/cm^2 at 2.42 V—calculated by using the free-space collected power of 5.1 nW and dividing by the total active device area of 12.6 μm^2. It is noteworthy that the abovementioned free-space collected power [and, thus, the intensity data shown in Figs. 1(a) and 5(a)] of the micro-LEDs developed here represents a conservative bound estimate of the externally emitted total power only, as our free-space collection did

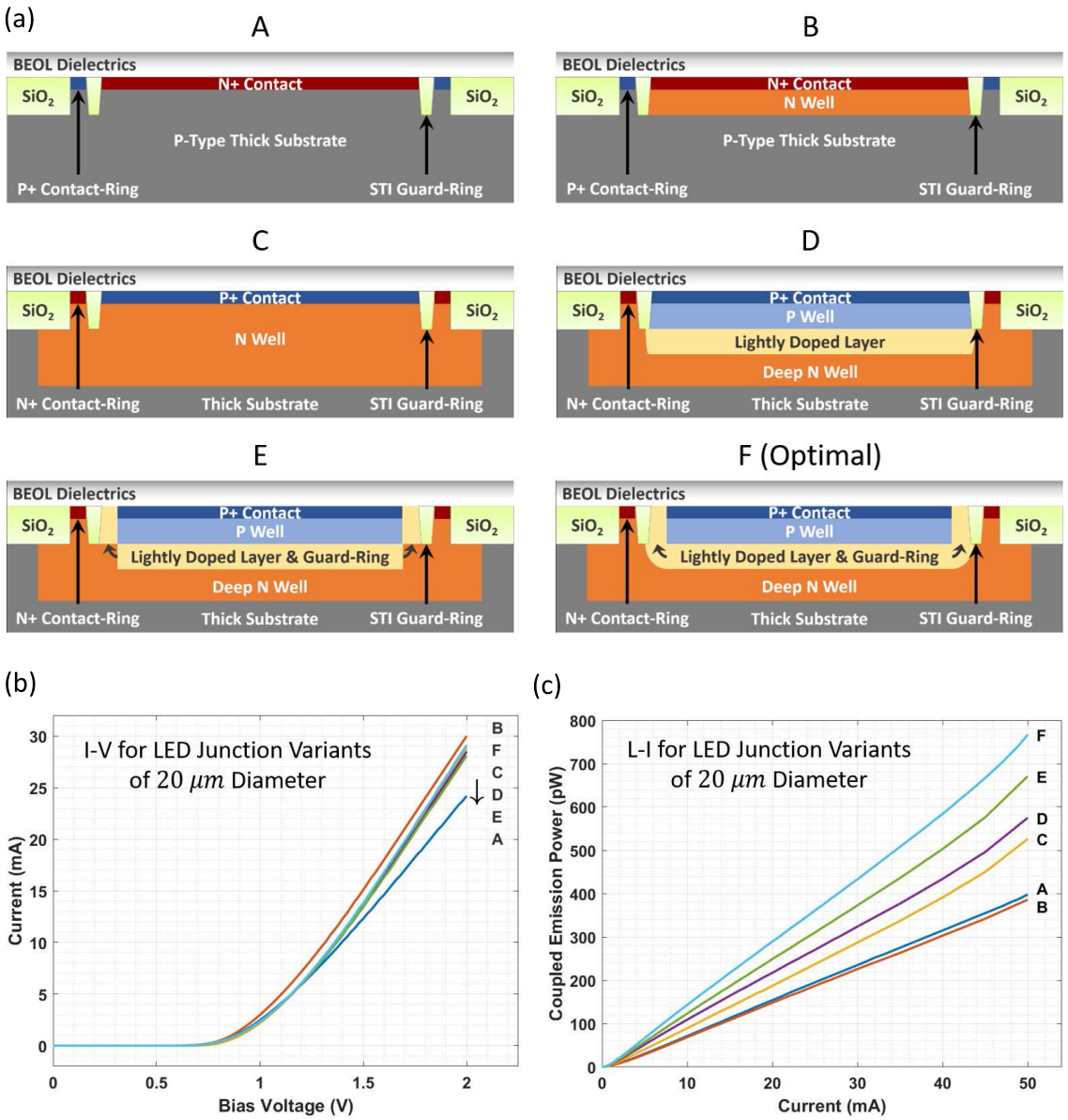

Fig. 4. (a) Schematic junction structures for the CMOS micro-LED design variants, with *F* being the optimal (identical to Fig. 2). (b) *I–V* curves for these design variants of 20-μm diameter. (c) *L–I* curves for these design variants of 20-μm diameter. For a fair comparison minimizing alignment inconsistency, all power measurements here from different micro-LED variants are butt-coupled to a standard 50-μm-core multimode fiber.

not collect all the LED emissions as would be the case, for example, using an integrating sphere.

Measurements were repeated on other junction variants of the LED design. These variants include n-p vertical junctions of different depths (designs A and B) and p-n junctions of different depths (designs C and D), as shown in Fig. 4(a). For the deep p-n junction design D, various lightly doped regions next to the STI guard ring were added, so as to suppress carrier diffusion to the silicon/STI interface where SRV can be large (designs E and F). According to the measured *I–V* and *L–I* curves of these junction variants, as shown in Fig. 4(b) and (c), respectively, we can see that the optimal junction (design F, identical to that in Fig. 2) produces more than double the optical power than the basic vertical junction (design A) at the same current but with lower bias voltage. This optimal design corresponds to a vertical p-n junction where the junction is as far from the top surface as possible (just over 1 μm). Likewise, the added lightly p-doped inner guard ring pushes the active recombination region away from the silicon/STI sidewalls, improves the radiative efficiency, and was observed to significantly enhance light emission from the outer perimeter of the devices.

C. Scaling Model for LEDs

Using the parameters introduced in Table I, we developed a simple model for the observed *L–I* characteristics. As all the measurements are performed under the steady-state (dc) condition, the conventional rate equations used to describe an LED reduce to coupled equations for the current density J and the external emission intensity I in terms of injected carrier density n

$$J = qt\left[\left(\frac{S_{\text{eff}}}{d}\right)n + An + Bn^2 + Cn^3\right] \tag{2}$$

$$I = \frac{P}{A_a} = Bn^2 \times t \times \eta_{\text{ex}} \times \langle h\upsilon \rangle \tag{3}$$

where q is the elementary charge, t is the active region thickness, d is the interface dimension of the device active region, P is the external emission power, η_{ex} is the photon extraction efficiency, and $\langle h\upsilon \rangle$ is the mean photon energy. It considered all the major recombination processes are introduced earlier and assumed that there is no leakage current.

Here, the goal is to use a model as simple as possible to reproduce the key features of device operation and extract any physical insight with minimal parameter fitting. By using widely accepted ABC parameters of silicon in the literature (as in Table I), the quality of the fit between the model and the measured data is most sensitive to the choice of active region thickness (t) and interface SRV (S_{eff}). A light extraction efficiency η_{ex} of 0.1% is assumed, which also aligns with what has been estimated in literature for similar devices [13]. The fitted active region thickness is 100 nm, and most importantly, to reproduce the curve splitting effect at the knees shown in Fig. 5 at around a current density of 10^2 A/cm^2, S_{eff} has to be $\sim 10^4$ cm/s. This extracted SRV is relatively low and contributes to the higher emission intensity of the present silicon micro-LEDs compared to devices that utilize lateral junctions near the silicon top surface without particular attention to passivation. The measured SRV is lower than most infrared emitting III–V semiconductors, such as GaAs and InP [5], [6], but still much higher than the best passivated silicon surfaces [1], indicating room for further improvement.

D. All-Silicon Optical Link

A simple optical link is demonstrated using the CMOS micro-LED emission with the multimode optical fiber coupling described above. We take advantage of the available light collection to demonstrate an all-silicon inter-chip optical link, as shown in Fig. 6(a).

We employ the long-wavelength optimized silicon Geiger-mode photodetector of 20-μm diameter discussed earlier. This single-photon avalanching detector (SPAD) is operated with an off-chip passive quenching circuit with a 100-kΩ quench resistance. The measured quench time was approximately 1.5 ns, and the measured reset time after a pulse was measured to be approximately 125 ns at -24.7 V and 50 ns at -26 V.

A CMOS LED of 20-μm diameter on one chip is modulated by a 0–1.6-V peak-to-peak square wave of 30% duty cycle. A CMOS SPAD on the other identical chip detects the modulated emission through a 5-m-long multimode fiber and produces a waveform of modulated photon detection counts (or probability) that tracks the transmitting signal. A typical modulation and detected waveform by oscilloscope are illustrated in the inset (middle) of Fig. 6(a). At 1-MHz (10-MHz) modulation, the extinction ratio (i.e., the ratio of photon counts during LED ON and OFF) was measured to be 5.66 (1.7) or 7.5 dB (2.3 dB). The modulation speed and the extinction ratio of the optical link are limited by the reset time and the DCR of the receiver, respectively.

To verify this hypothesis, we replaced the receiver side of the link with a commercial photon counting module also utilizing a silicon SPAD but with an active-quenching circuit (Excelitas SPCM-EDU). This SPAD is packaged with a fiber connector, the module has a lower DCR of 0.26Hz/μm^2, and the active quenching circuit has a faster reset time of 35 ns. Fig. 6(b) summarizes and compares the measured extinction ratio for using either the on-chip SPAD or the commercial photon counting module as a function of LED modulation frequency. In the latter case, the measured extinction ratio is 21.3 dB at 1 MHz and 3.7 dB at 250 MHz, respectively. Further improvements of the on-chip SPAD along with an integration of the on-chip quenching circuit should allow for higher speeds and improved extinction ratios. These data, however, demonstrate the feasibility of modulating a forward-biased CMOS micro-LED at speeds between 1 and 250 MHz. It is worth noting that the highest LED modulation frequency of 250 MHz demonstrated here is limited by the speed of the signal generator (Agilent 81180A arbitrary waveform generator). The extinction ratio and signal-to-noise ratio are limited by fiber coupling efficiency and detector.

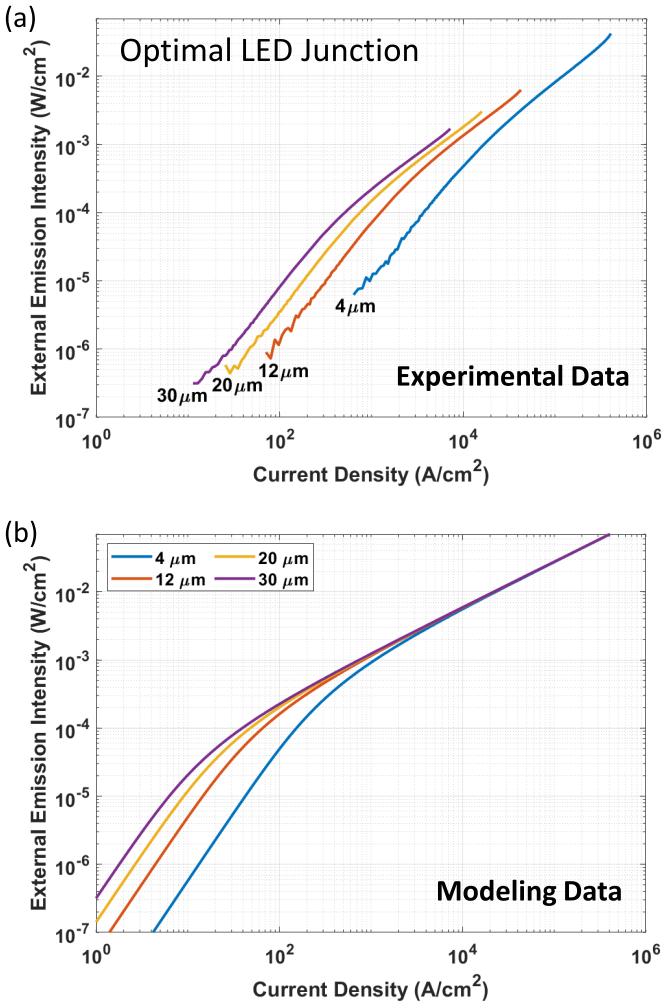

Fig. 5. (a) Experimental data of external emission intensity versus current density for the optimal LED junction (structure F) of different active region diameters. The intensity of the 4-μm device is directly measured by 0.95-NA objective lens via free-space collection. The others are derived from their fiber-coupled power and correct for fiber coupling efficiency. (b) Simulation data from a simple rate equation modeling aiming to reproduce features in (a) with minimal parameter fitting.

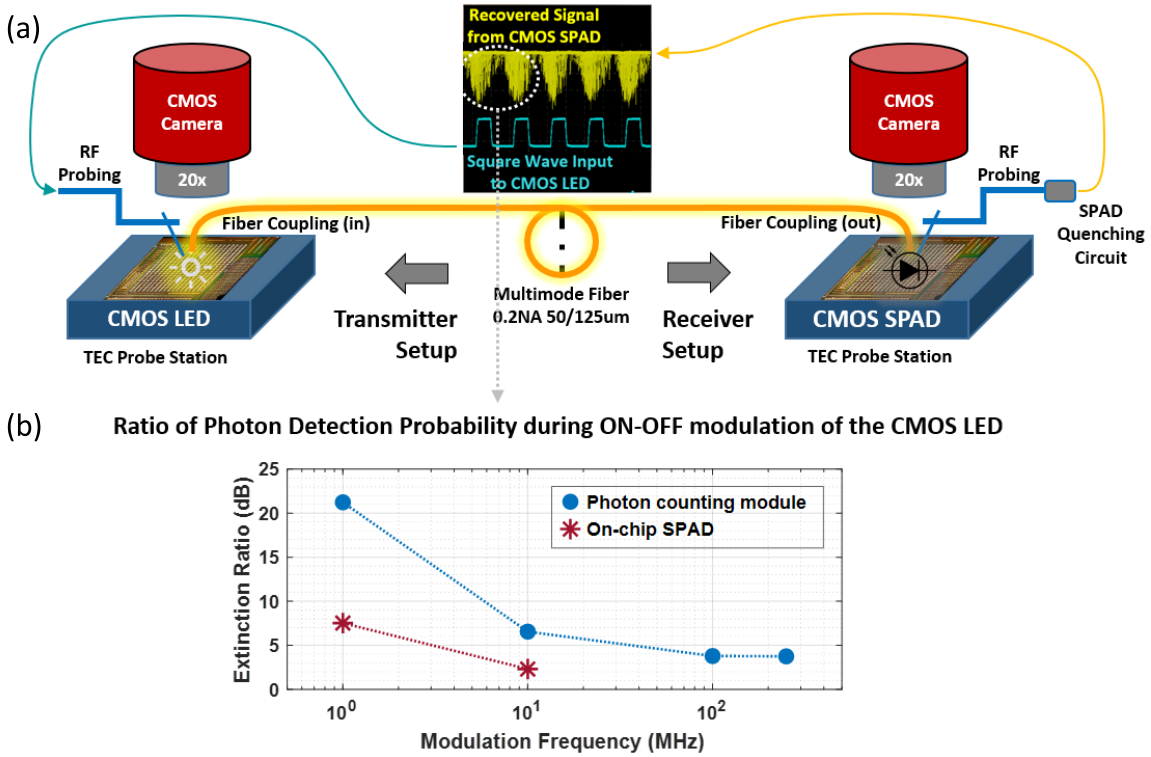

Fig. 6. (a) Schematic of a chip-to-chip optical interconnect utilizing only CMOS devices. Optical transmission of modulation waveforms from a CMOS LED (20-μm diameter) to a CMOS SPAD (20-μm diameter) over a 5-m-long standard multimode optical fiber is shown in the inset. The optical fiber is directly coupled to both the CMOS LED and the SPAD without using an objective lens or other optics. (b) Observed ratio of photon detection counts during ON–OFF modulation of the CMOS LED. Results by the on-chip SPAD and a commercial photon counting module are compared.

IV. Conclusion

This article presents results on a low-voltage, high-brightness micro-LED realized in a 55-nm BCDLite process. This article reports the first forward-biased CMOS LEDs with vertical junctions and the first CMOS LEDs to achieve sufficiently high brightness at low voltage for useful fiber coupling and detection. The device is manufactured directly in commercial microelectronic CMOS technology without any modification or postprocessing, along with other photonic and electronic components integrated on the same chip. Given the useful intensity at technologically important NIR wavelength, scalable planar architecture, and compatibility with the microelectronic CMOS process, such a native light emitter is an important building block for silicon electronic-photonic integration.

Further development of CMOS LEDs complements the broad range of silicon photonic devices that are available in modern foundry processes. These devices enable chip-sized systems for applications ranging from proximity sensors and time-of-flight sensors to optocouplers and data links.

Acknowledgment

The authors are grateful for the die packaging assistance from Dr. William Loh and Lincoln Labs, which allowed characterization experiments to continue during the COVID-19 pandemic.

References

[1] R. S. Bonilla, B. Hoex, P. Hamer, and P. R. Wilshaw, "Dielectric surface passivation for silicon solar cells: A review," *Phys. Status Solidi (A)*, vol. 214, no. 7, Jul. 2017, Art. no. 1700293, doi: 10.1002/pssa.201700293.

[2] T. Trupke and M. A. Green, "Temperature dependence of the radiative recombination coefficient of intrinsic crystalline silicon," *J. Appl. Phys.*, vol. 94, no. 8, pp. 4930–4937, Oct. 2003, doi: 10.1063/1.1610231.

[3] D. K. Schroder, "Carrier lifetimes in silicon," *IEEE Trans. Electron Devices*, vol. 44, no. 1, pp. 160–170, Jan. 1997, doi: 10.1109/16.554806.

[4] K. A. Bulashevich and S. Y. Karpov, "Impact of surface recombination on efficiency of III-nitride light-emitting diodes," *Phys. Status Solidi, Rapid Res. Lett.*, vol. 10, no. 6, pp. 480–484, Jun. 2016, doi: 10.1002/pssr.201600059.

[5] R. K. Ahrenkiel, R. Ellingson, S. Johnston, and M. Wanlass, "Recombination lifetime of $In_{0.53}Ga_{0.47}As$ as a function of doping density," *Appl. Phys. Lett.*, vol. 72, no. 26, pp. 3470–3472, Jun. 1998, doi: 10.1063/1.121669.

[6] D. K. Schroder, *Semiconductor Material and Device Characterization*. Hoboken, NJ, USA: Wiley, 2015, doi: 10.1002/0471749095.

[7] M. A. Green, J. Zhao, A. Wang, P. J. Reece, and M. Gal, "Efficient silicon light-emitting diodes," *Nature*, vol. 412, no. 6849, pp. 805–808, Aug. 2001, doi: 10.1038/35090539.

[8] V. Agarwal *et al.*, "Optocoupling in CMOS," in *IEDM Tech. Dig.*, Dec. 2018, pp. 32.1.1–32.1.4, doi: 10.1109/IEDM.2018.8614523.

[9] S. Dutta, R. J. E. Hueting, A.-J. Annema, L. Qi, L. K. Nanver, and J. Schmitz, "Opto-electronic modeling of light emission from avalanche-mode silicon p+n junctions," *J. Appl. Phys.*, vol. 118, no. 11, Sep. 2015, Art. no. 114506, doi: 10.1063/1.4931056.

[10] H.-C. Lee and C.-K. Liu, "Si-based current-density-enhanced light emission and low-operating-voltage light-emitting/receiving designs," *Solid-State Electron.*, vol. 49, no. 7, pp. 1172–1178, Jul. 2005, doi: 10.1016/j.sse.2005.04.008.

[11] W. Wang, B.-J. Huang, Z. Dong, and H.-D. Chen, "Multifunctional silicon-based light emitting device in standard complementary metal—Oxide—Semiconductor technology," *Chin. Phys. B*, vol. 20, no. 1, Jan. 2011, Art. no. 018503, doi: 10.1088/1674-1056/20/1/018503.

[12] J. M. Smith *et al.*, "Comparison of size-dependent characteristics of blue and green InGaN microLEDs down to 1 μm in diameter," *Appl. Phys. Lett.*, vol. 116, no. 7, Feb. 2020, Art. no. 071102, doi: 10.1063/1.5144819.

[13] S. Dutta, G. J. M. Wienk, R. J. E. Hueting, J. Schmitz, and A.-J. Annema, "Optical power efficiency versus breakdown voltage of avalanche-mode silicon LEDs in CMOS," *IEEE Electron Device Lett.*, vol. 38, no. 7, pp. 898–901, Jul. 2017, doi: 10.1109/LED.2017.2701505.