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High-speed polysilicon CMOS photodetector for telecom and datacom

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Absorption by mid-bandgap states in polysilicon or heavily implanted silicon has been previously utilized to implement guided-wave infrared photodetectors in CMOS compatible photonic platforms. Here, we demonstrate a resonant guided-wave photodetector based on the polysilicon layer that is used for the transistor gate in a microelectronic SOI CMOS process without any change to the foundry process flow ("zero-change" CMOS). Through a combination of doping mask layers, a lateral pn junction diode in the polysilicon is demonstrated with a strong electric field to enable efficient photo-carrier extraction and high-speed operation. This photodetector has a responsivity of more than 0.14 A/W from 1300 to 1600 nm, a 10 GHz bandwidth, and 80 nA dark current at 15 V reverse bias. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4962641]

The increasing demand for higher data rate interconnects at datacenters and communications for the metro has recently driven the research and development on terabit interconnect technologies.[1] CMOS and CMOS-compatible photonics are posited to be viable solutions for these systems as they enable large-scale integration of high-speed and low-power optical transmitters and receivers with different multiplexing schemes at a low cost. The same device technology can also address gigabit passive optical networks for fiber-to-the-home (FTTH) application that are growing at a rapid pace.[2] Recent progress in zero-change CMOS photonics in the 45 nm SOI CMOS node has enabled the first microprocessor with monolithic optical transceivers for communication with the memory.[3] This is the same process used for the manufacturing of high performance processors in supercomputers[4] and microprocessors for the consumer market such as the Playstation 3 Slim's Cell Broadband engine.[5] With the possibility for monolithic integration of electronics with photonics at the manufacturing cost and scale of consumer electronics, this integration approach has the potential for a significant impact in the optical datacom and telecom space.

Today, zero-change, deep submicron, CMOS photonics delivers high performance passive and active individual photonic components such as low loss waveguides and high Q resonators,[6] high efficiency vertical grating couplers (<0.5 dB insertion loss),[7] high-speed and compact depletion-mode modulators,[8] and highspeed (32 GHz @ 0.02 A/W)[9] and high quantum efficiency SiGe photodetectors (5 GHz @ 0.55 A/W).[10] The unique advantage of monolithic integration with electronics has enabled low-power transmitters (30 fJ/bit) and receivers (374 fJ/bit), and wavelength locking of the resonant filters and modulators.[11] The combination of these devices and sub-systems enabled the first microprocessor to memory optical interconnect with 1.3 pJ/bit on-chip energy consumption.[3] The main hurdle towards the extension of this device platform to the datacom and telecom spaces has been the lack of a high-speed detector at wavelength standards for these applications

(i.e., from 1300 to 1550 nm). The monolithic SiGe photodetectors in this platform used so far for inter-chip interconnect application have high bandwidth and quantum efficiency[9,10] but their operation is limited to wavelengths below 1200 nm due to the small mole fraction of Ge in CMOS.

Another mechanism that has been used to implement infrared photodetectors in CMOS compatible platforms is absorption by the defect states in silicon or polysilicon.[12–19] Defects can generate energy states inside the bandgap of silicon and assist absorption of infrared photons. Optical absorption is observed in moderately doped guided-wave silicon devices with pn junctions through the defects generated during ion implantation;[12] and silicon has been intentionally implanted at high dosages (10^{13} to 10^{14} cm^{-2}) to introduce defects and increase the quantum efficiency of these photodetectors.[13–15] Resonant detectors using this technique have achieved responsivities in the range of 0.1 to 0.2 A/W with a few GHz bandwidth.[13,14] A waveguide detector was also demonstrated with a responsivity as high as 6–10 A/W with 35 GHz at 20 V bias bandwidth by optimizing the anneal condition for activation of the defect states.[15] As reported separately in Refs. 13 and 15, these devices require a break-in at high current density to change the state of the silicon defects to increase their quantum efficiency. The state of the defects will also be reversed by heating the device to only 250 °C for a few seconds.[15] These effects raise reliability issues when building telecom or datacom systems. On the other hand, polysilicon with grain boundary midgap states has been used for building photodetectors and have achieved comparable or better performance compared to ion-implanted silicon resonant photodetectors without these reliability concerns.[16–19] Polysilicon detectors at 1280 nm and 1550 nm with a responsivity of 0.2 A/W (at 2.5 V) with 8 GHz bandwidth (at 10 V bias) are already demonstrated in a modified bulk CMOS[17] and have been used to demonstrate the first optical link using monolithic optical transmitters and receivers in a bulk CMOS process.[20] Also, polysilicon exists in the majority of CMOS processes as the gate for FETs, and as is shown in this work, can be used to implement high performance photodetectors without changes to the foundry CMOS processes. Therefore, we believe that

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polysilicon is a promising and reliable material for implementing photodetectors for interconnect and telecommunication applications.

We recently used the gate polysilicon in GlobalFoundry's (formerly IBM's) 45 nm CMOS SOI process to implement an infrared photoconductor at telecom and datacom wavelengths.[19] We demonstrated a resonant photodetector and were able to achieve 0.34 A/W responsivity at 25 V forward bias and 1 GHz bandwidth at bias voltages above 5 V. Because of predoping in the polysilicon gate associated with all advanced CMOS processes for avoiding gate depletion,[21] we were not able to achieve a true lateral pn diode, and as a result, that device behaved as a photoconductor. Because of the weak electric field in the absorption region, the device had poor photocarrier collection and a slow response. We should note that the implementation of diodes for optical detectors and modulators in polysilicon requires careful calibration of the doping concentration due to the high density of defects that can trap carriers and considerably lower carrier activation until the defect states are occupied.[22] This is particularly important for optical devices as they require activated carrier concentrations of a few 10^{18} cm^{-3}, which is close to the doping concentration ($\sim 10^{18}$ cm^{-3}) where the onset of carrier activation in polysilicon occurs.[22] Despite these complexities and the lack of flexibility for adjusting doping concentrations in a zero-change process, a lateral pn junction diode is realized here through a combination of doping layers and counter-doping the polysilicon gate. This has enabled a high-speed zero-change CMOS infrared detector with a responsivity of 0.14–0.2 A/W from 1300 to 1600 nm with a 3 dB bandwidth of 10 GHz under 15 V reverse bias.

Figure 1(a) shows the cross-section of the photodetector waveguide, which will eventually be used to form a resonant microring photodetector (Fig. 1(c)). The crystalline body silicon layer, which is normally used to implement the transistor channel and source/drain, and the gate polysilicon layer are both used in the design of the detector. The thickness of both layers is below 100 nm in this process. The optical mode of the ring is laterally confined using the body silicon ridge (600 nm wide), which also helps to reduce the optical loss by pulling the mode away from the rough surface of the polysilicon. The contour lines of the transverse electric (TE) mode at 1550 nm are super-imposed on the device cross-

section in Fig. 1(a). The confinement factor of this mode in polysilicon is roughly 0.3.[19] The absorbing material is the polysilicon gate layer that is predoped either n or p for the NFETs and PFETs in this process.[21] Using a combination of doping mask layers, we were able to counter-dope one type of predoping and implement a lateral p+pn+ junction in the polysilicon layer. The width of the p region (W_p) is 0.8 μm in this design. A resonant microring detector with a diameter of 24 μm is designed to increase the interaction length for a more compact device. The device was implemented using our photonic design software[23] and was fabricated in Global Foundry's 45 nm SOI CMOS process. Details on the resonator design and substrate release process used for these SOI devices with thin buried oxide layer can be found in Ref. 6. Figure 1(b) shows the defect photodetector block on the CMOS die from the front side (total of 36 detectors) and Fig. 1(c) shows the optical micrograph of one of the microring detectors through the backside of the die after the substrate is released and before transfer onto the glass substrate. Since the input/output grating couplers and waveguides are implemented in the low-loss body silicon layer, we use a taper in polysilicon to gradually transition the optical mode from the body silicon waveguide to the body/poly hybrid detector region (see Fig. 1(c)).

The top plot in Fig. 2(a) shows the transmission spectrum of a resonant mode of the microring detector near 1550 nm with a loaded Q of approximately 2000 with 10 dB of optical extinction (close to critical coupling). Equivalent propagation loss is 130 dB/cm. The free-spectral range of the device is 9.4 nm. The bottom plot shows the photocurrent as the light is coupled into the resonator under 15 V reverse bias. The wavelength of the laser is tuned to this resonance and the I–V curves under dark and illumination by ~ 15 μW optical power in the waveguide are obtained (Fig. 2(b)). We obtained 80 nA dark current and ~ 2 μA photocurrent corresponding to a 0.15 A/W responsivity at 15 V reverse bias. The responsivity-bias curve of the device is shown in the inset. We repeated this measurement over a large wavelength range from 1300 to 1600 nm and calculated the responsivity of the device. As seen in Fig. 2(c), the device exhibits a responsivity between 0.14 and 0.2 A/W in this wavelength range. The extinction ratio of the resonator changes across this wavelength range from 3 dB at 1310 nm to higher than 10 dB for wavelengths above 1500 nm. This is mainly due to
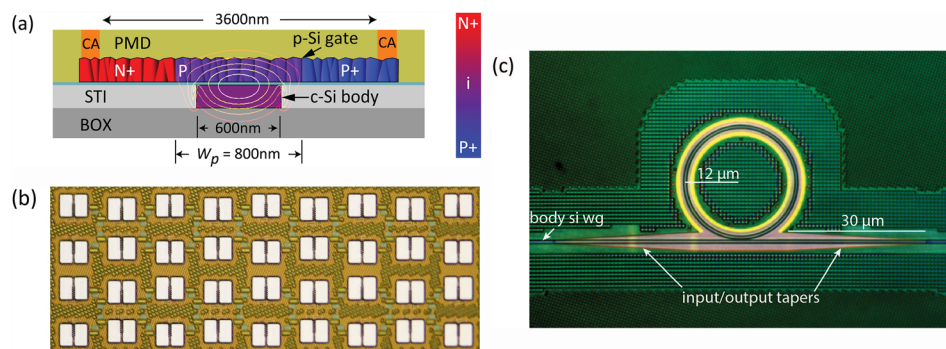

FIG. 1. (a) Schematic of the cross-section of the detector showing the inverse ridge structure and the diode junction. The contour lines of the Poynting vector of the waveguide TE mode along the direction of propagation are superimposed. PMD: pre-metal dielectric; CA: contact; c-Si: crystalline silicon; STI: shallow trench isolation; BOX: buried oxide. (b) Optical micrograph of the defect detector block on the CMOS chip. (c) Optical micrograph of the microring photodetector with the input/output polysilicon taper regions. The polysilicon film covers the entire ring and the waveguide-resonator coupling region. Polysilicon appears pink in the figure.
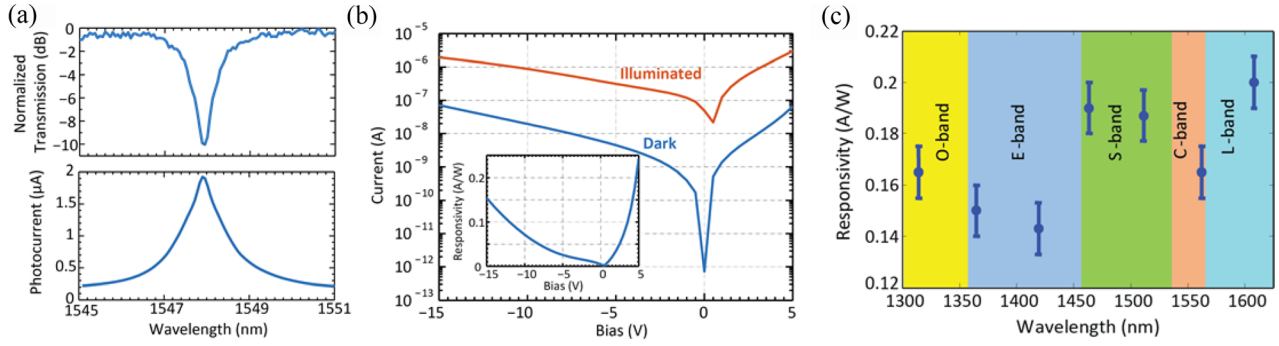
FIG. 2. (a) Top and bottom plots show the normalized transmission response and photocurrent of the microring photodetector for a resonance near 1550 nm. (b) I–V curves of the polysilicon microring photodetector under dark (blue curve) and illumination with 15 μW optical signal in the waveguide at the resonance wavelength of the device (red curve). Inset: responsivity of the photodetector as a function of bias voltage under 15 μW optical signal in the waveguide. (d) Responsivity of the photodetector under 15 V reverse bias from 1310 to 1610 nm.

the change of the coupling condition across such large wavelength range and, to a lesser extent, the cavity Q. Based on the extracted Q and coupling coefficients at every wavelength in Fig. 2(c), the finite power drop in the microring across this wavelength span is compensated for and the responsivity of a critically coupled microring is estimated to be $R_{critical} = R_{measured} [2 - (\lambda(\text{nm}) - 1310)/300]$, where $R_{measured}$ is the value reported in Fig. 2(c). For this measurement, we adjusted the laser power such that the optical power in the resonator is fixed for every wavelength in Fig. 2(c). This is important because of the optical power dependence of responsivity and the inevitable wavelength dependence of the grating coupler insertion loss, waveguide-resonator coupling, and resonator Q over the entire 300 nm wavelength span (see Ref. 19). We attribute the variation of responsivity in this wavelength range to the wavelength dependent loss of the dielectric films that are deposited on top of the device[6] and to the inability to maintain critical coupling across the 300 nm span with a single waveguide-resonator coupling gap.

Although the turn-on voltage of the device is above 5 V forward bias, the high quantum efficiency and large bandwidth of the device (as will be discussed later), which are on a par with polysilicon detectors demonstrated in custom processes,[17] are good indications that the device behaves as a pn

diode under the reverse bias with a strong electric field in the depletion region. The dimension of the depletion region was confirmed by the measurements of the reverse current behavior as a function of the p region (W_p) width. Through doping conductivity test structures, we know that the p+ and n+ regions have a carrier concentration of at least an order of magnitude higher than the center p region. As a result, we expect that the depletion region to be almost entirely in the p region. As the reverse bias and consequently the electric field are increased in the p region, current will be enhanced through the Poole-Frankel (PF) barrier lowering at the defects in polysilicon. This effect has been observed and studied previously in polysilicon pn diodes.[24] The enhancement of the reverse current is given by

$$I_{PF} = I_0 \exp\left(q\beta_{PF}\sqrt{E_{dep}}/KT\right)$$
$$= I_0 \exp\left(\frac{q\beta_{PF}}{KT\sqrt{W_{dep}}}\sqrt{V}\right), \quad (1)$$

where β_{PF} is the PF coefficient in polysilicon, V is the reverse bias voltage, q is the charge of electron, and E_{dep} and W_{dep} are the E-field and the width of the depletion region. From Equation (1), we have $ln(I_{PF}) = ln(I_0) + (q\beta_{PF}/\sqrt{W_{dep}})\sqrt{V}$, which indicates that the slope of the $ln(I_{PF})$ versus $\sqrt{V}$ is
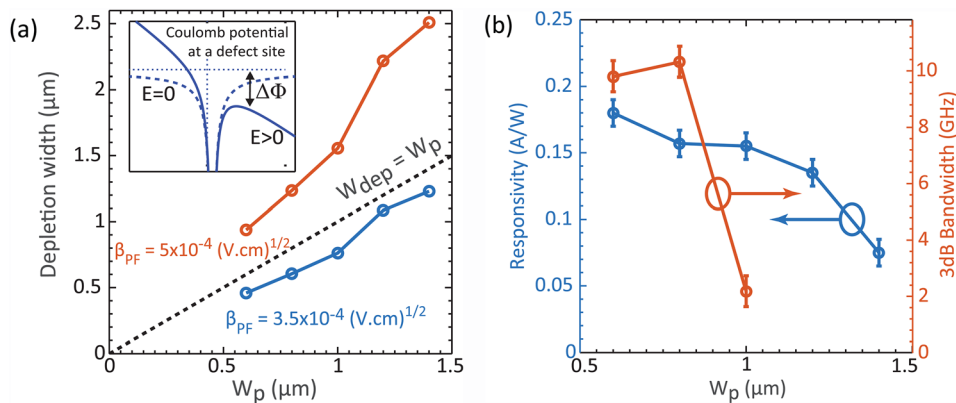

FIG. 3. (a) W_{dep} estimated based on PF model for different widths of the p doped region W_p. Red and blue curves show the results for the maximum and minimum of the PF coefficient (β_{PF}) reported for polysilicon in Ref. 24. The dashed line shows W_p on the vertical axis to help visualize the comparison between the estimated W_{dep} vs. W_p. The inset shows the mechanism of Poole-Frenkel effect. The dashed and solid lines represent the Coulombic potential without and with an electric field. $\Delta\phi$ is the potential barrier lowering due to the electric field. (b) Responsivity and 3 dB bandwidth of the polysilicon detector as a function of the width of the low doped region (W_p).
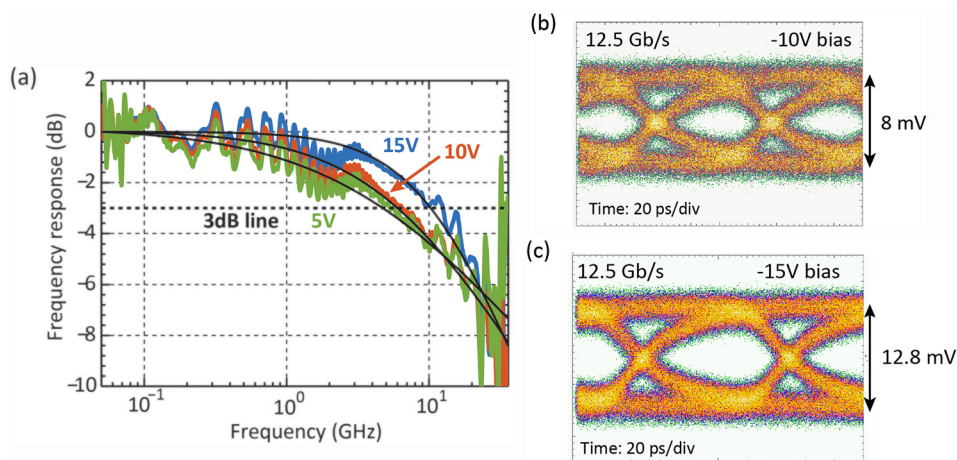
FIG. 4. (a) Frequency response of the polysilicon photodetector under -15 V (blue curve), -10 V (red curve), and -5 V (green curve) biases at 1550 nm. (b) and (c) The eye diagrams of the photodetector at 12.5 Gb/s under 10 V and 15 V biases, respectively.

proportional to $q\beta_{PF}/(KT\sqrt{W_{dep}})$. We can use this relationship and the previously characterized β_{PF} in polysilicon[24] to estimate W_{dep}. We have designed five devices with different W_p from 0.6 μm to 1.4 μm, and for each device, we estimated the lower and upper bounds for W_{dep} using the minimum and maximum β_{PF} reported for polysilicon in Ref. 24 ($3.5 \times 10^{-4}(\text{V cm})^{1/2}$ and $5 \times 10^{-4}(\text{V cm})^{1/2}$). The result is shown in Fig. 3(a), in which the red and blue curves show the upper and lower bounds of W_{dep} estimated through the approach explained above plotted against the physical dimension of the predoped p-region, W_p. It is observed that the estimate of W_{dep} follows W_p to a good degree. Although the value of β_{PF} in our material is not independently determined, the relative scaling of W_{dep} and W_p and close agreement for the lower bound of β_{PF} is a good indication that the depletion width is close to W_p and that there is a strong electric field inside the p region in the reverse bias assisting the collection of photo-generated carriers. The responsivity and RF bandwidth of devices with different W_p are also plotted in Fig. 3(b) at 15 V reverse bias.

We also measured the frequency response of this detector using a vector network analyzer and a lithium niobate electro-optic modulator to transfer the RF signal to the optical carrier. The results are shown in Fig. 4(a) at different bias conditions. It is observed that the device has a 3 dB bandwidth of 5 GHz, 8 GHz, and 10 GHz, under 5 V, 10 V, and 15 V reverse bias, respectively. To confirm the performance of this device for high data-rate digital communications, we obtained eye diagrams by measuring the photocurrent for a $2^{31}-1$ bit pseudorandom binary sequence (PRBS) optical signal. Figures 4(b) and 4(c) show the eye diagrams for a 12.5 Gb/s PRBS signal under 10 V and 15 V biases, respectively, showing completely open eyes at this data-rate. We expect our device to be fast enough to detect 20 Gb/s non-return-to-zero (NRZ) signals based on its 3 dB bandwidth. The fast device response along with the broad spectral bandwidth makes the device appealing for a range of high data-rate interconnect and communication applications such as Ethernet, FTTH, and telecommunications.

Further improvements, especially in the operating voltage, can be implemented. The fact that the device does not exhibit a clear forward turn-on below 5 V indicates that the junction is not optimized. This is most likely because multiple ion-implantations with different polarities (e.g., source/

drain halo and extension) and implant conditions (e.g., angle) are associated with a single mask layer in the 45 nm SOI process used for this work. We believe that this has resulted in a complex diode structure that requires larger voltages to achieve full depletion. We have previously shown that with an optimized diode junction it is possible to achieve quantum efficiencies of more than 15% with only 2.5 V.[17] Through a combination of different doping masks, it is likely that an optimized diode junction with a strong built-in electric field lowers the operating voltage of the detector demonstrated in this work to a few volts without degrading quantum efficiency and bandwidth.

In conclusion, we have demonstrated a high-speed photodetector in zero-change CMOS with 10 GHz bandwidth that covers the entire telecom and datacom wavelength range with a responsivity of more than 0.14 A/W for communications applications. This device combined with the monolithic receiver circuits, optical transmitters, efficient thermo-optic tunable elements with wavelength stabilization circuits that are already demonstrated in the same process[11] can enable single-chip transceiver solutions at the cost and scale of consumer electronics.

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