Sub-bandgap polysilicon photodetector in zero-change CMOS process for telecommunication wavelength

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Abstract: We report a defect state based guided-wave photoconductive detector at 1360-1630 nm telecommunication wavelength directly in standard microelectronics CMOS processes, with zero in-foundry process modification. The defect states in the polysilicon used to define a transistor gate assists light absorption. The body crystalline silicon helps form an inverse ridge waveguide to confine optical mode. The measured responsivity and dark current at 25 V forward bias are 0.34 A/W and 1.4 μA, respectively. The 3 dB bandwidth of the device is 1 GHz.

OCIS codes: (250.0250) Optoelectronics; (040.5160) Photodetectors.

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1. Introduction

Recently, there has been significant progress on electro-optic interfaces directly in microelectronic CMOS processes [1–3]. When such photonic integration is realized with no in-foundry

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process modifications, it is possible to realize large-scale optoelectronic systems, with the potential to impact applications ranging from microprocessor-to-memory interfaces [3], high-speed signal processing [4], and high-performance sensors [5].

Substantial progress has been made in the development of optical interconnects based on photonic components monolithically integrated with 45 nm CMOS microelectronics using no process changes. Complete optical links have been demonstrated with 30 fJ/bit transmitters and 374 fJ/bit receivers with 6 μA peak to peak photocurrent sensitivity at 5 Gb/s data rates [6]. These optical links exploit low-loss waveguides with propagation losses of less than 5 dB/cm in the 1170 nm-1250 nm range [7], resonant modulators with interleaved diode junctions operating with 5 fJ/bit with 1.5 dB insertion loss and 8 dB extinction ratio at 1180 nm [8], and high speed SiGe photodetectors with 32 GHz bandwidths at 1 V bias [9]. The operating wavelength for the optical interconnect in [6] is optimized for the SiGe waveguide detectors and is restricted to wavelength shorter than 1200 nm. In standard CMOS process, SiGe is used for strain engineering. The Ge content is estimated to be 25% to 35% [9]. Such a SiGe alloy is not capable of detecting 1550 nm light. While these device and interconnect results represents progress for monolithic electronics-photonics integration, the only photonic materials that have been available in microelectronics CMOS are crystalline Silicon and strained SiGe. While the wavelength restriction may not be significant for intra-chip communications or for board-level interconnects, this is a significant barrier for important applications such as telecommunications where 1550 nm EDFAs define the choice of wavelength or for Ethernet applications such as data centers where 1310 nm is required for interoperability [10].

Extending the infrared sensitivity of CMOS detectors can have important applications even at modest speeds. For example, Fiber-to-the-home (FTTH) requires high-volume production and monolithic CMOS may provide a cost-effective solution [11]. Widely deployed GPON standards for FTTH require link speeds of only 1 Gbps at 1310 nm and 1550 nm. Additionally, extending the detection wavelength of a CMOS sensor is of broad interest [12–14]. Previous efforts to extend the infrared range of CMOS imagers to around 1250 nm has used thin-film photosensitive materials [12] but there are currently no low-cost image sensor solution at longer wavelengths. By connecting an array of vertical grating couplers [5] to the detectors presented here, it is possible to make an infrared camera in CMOS using waveguide IR photodetectors. Such a detector array could be used for low cost infrared LIDAR system and spectroscopy as well [15].

Here, we report the first 1360-1630 nm detectors integrated in zero-change CMOS. We overcome the severe material constraints of zero-change by exploiting absorption that results from mid-gap states in the polysilicon film used for the transistor gate. An illustration of sub-bandgap absorption is shown in Fig. 1(a). With the assistance from defect states, photons with energy less than the bandgap can generate electron-hole pairs. There have been many recent demonstrations of defect state based photodetectors. Ion implantation is a common method to introduce damage in crystalline silicon [16–19]. Additionally, surface state absorption assists sub-bandgap absorption as well [20]. Defect doping by ion implantation to increase the 1550 nm response of silicon photodetectors is a possible solution but requires some modifications to the standard CMOS microelectronics process.

Here, we report 1550 nm detectors that exploit the gate polysilicon. There are several significant challenges to using this layer for absorption. First of all, high surface roughness associated with the columnar grain growth for the gate polysilicon will introduce high scattering loss [21]. A TEM of cross section of a polysilicon waveguide is shown in Fig. 1(b). The measured surface roughness of polysilicon is around 6-8 nm rms with a correlation length of 100-200 nm [22]. Secondly, the thickness of polysilicon film is smaller than 100 nm [21]. Additionally, mid-gap states have a small absorption cross-section. Finally, pre-doping is employed to prepare the

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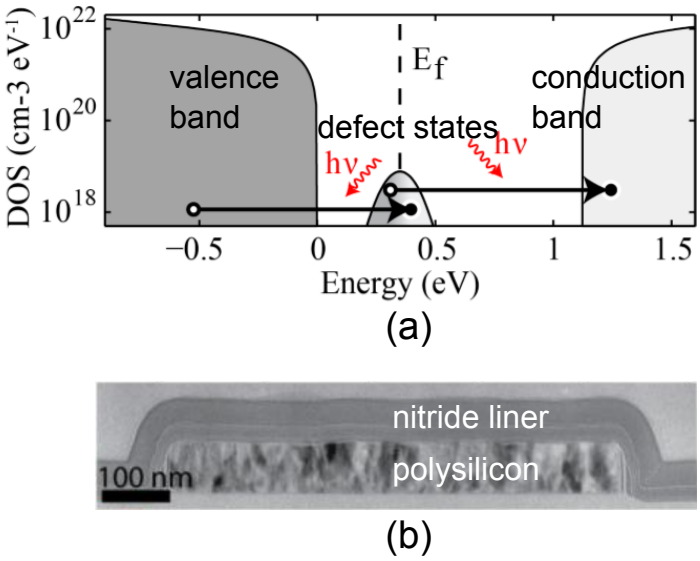

Fig. 1. (a) Polysilicon density of states (DOS) showing defect states in polysilicon assisting sub-bandgap photon absorption and electron-hole pairs generation [22]. (b) Transmission electron micrograph of gate polysilicon showing the grain structure and the surface roughness [21].

deposited polysilicon for self-aligned implant of both p-type and n-type MOSFETs [23, 24].

We have previously demonstrated detectors using the columnar gate polysilicon in a photonics-optimized process [25]. In that work, CMP was used to remove the surface roughness, the film thickness was increased to 220 nm and no pre-doping existed for the gate polysilicon. In this way, we were able to realized waveguides with 10 dB/cm loss at 1280 nm. Resonant photodetectors were constructed from this polysilicon to yield 20% QE detectors with 10 GHz bandwidth that could be integrated with CMOS receivers. This optimized columnar gate polysilicon yielded high performance detectors from 1280 nm to 1550 nm. The degree of process modification that was required to yield such devices is not available if we are to exploit a state-of-the-art CMOS processes that are capable of yielding the billions of transistors required for microprocessors, graphics processors, digital switch fabrics, or digital signal processors.

In order to overcome the challenges presented above, we propose an alternate design strategy that can be implemented in zero-change CMOS. To overcome the surface roughness and the small film thickness, we implement ridge waveguides where the optical mode is confined primarily in the crystalline silicon body layer. This allows us to route signals on the chip in the low-loss crystalline silicon waveguide and couple to the polysilicon only at the photodetectors. As the gate polysilicon experiences a high-density pre-doping implant, it is not possible to introduce a true intrinsic region for a p-i-n junction. Instead, we construct a photoconductive detector that exploits conductance modulation by the photo-generated carriers. Finally, the quantum efficiency is enhanced by constructing resonant micro-rings in the polysilicon/crystalline silicon ridge waveguides.

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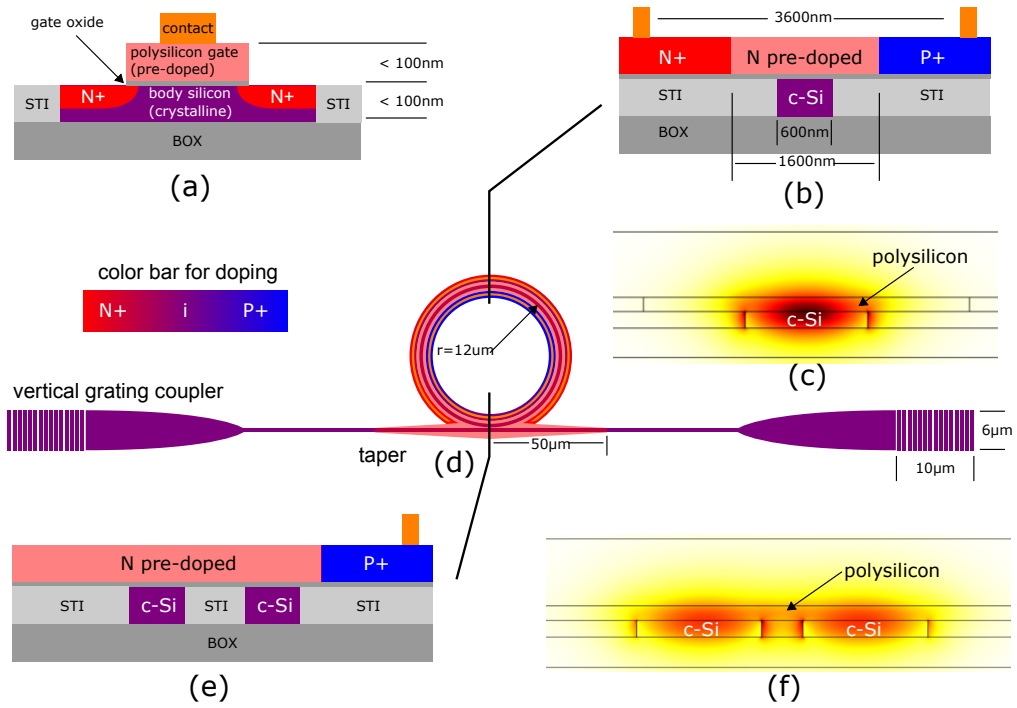

Fig. 2. (a) Cross-section of a typical n-type MOSFET in SOI CMOS. (b) Cross-section of an inverse ridge waveguide formed by polysilicon cap and crystalline silicon ridge. (c) Mode profile of the inverse ridge waveguide. (d) Bird's eye view of the micro-ring photodetector. Tapers are used to reduce coupling loss between crystalline silicon waveguide and inverse ridge waveguide. Vertical grating couplers are used to couple light with off-chip fibers.(e) Cross section of the coupling region. The gap size between two crystalline silicon ridge determine the coupling strength. (f) Mode profile of the coupling region.

2. Device Design

Figure 2(a) shows the schematic of an n-type MOSFET in the partially depleted SOI CMOS process. The thickness of body silicon and gate polysilicon layers are less than 100 nm and they are separated by a thin layer of gate oxide. We have shown previously that it is possible to implement low-loss integrated optical devices in this platform by removing the silicon substrate under the waveguides [8, 9, 21]. For the design of the photodetector, we can use a combination of the body and gate layers (both are patternable in the SOI process) to confine the optical mode and we can implement metal contacts on the the polysilicon gate layer to extract the photo-generated carriers. In order to improve the quantum efficiency of the photodetector, we have to minimize two main sources of optical loss: metal loss by field overlap with the metal contacts on polysilicon, and scattering loss by the roughness on the top surface of polysilicon.

Here, an inverse ridge waveguide is introduced to address these design criteria. Figure 2(b) shows the cross-section of this waveguide structure. In this design, the body silicon is used to laterally confine the optical mode to avoid field overlap with the metal contacts on polysilicon and also pull the mode away from the top surface of the polysilicon. As shown in Fig. 3(a), the field confinement above polysilicon drops for a body silicon width above 200 nm while the field

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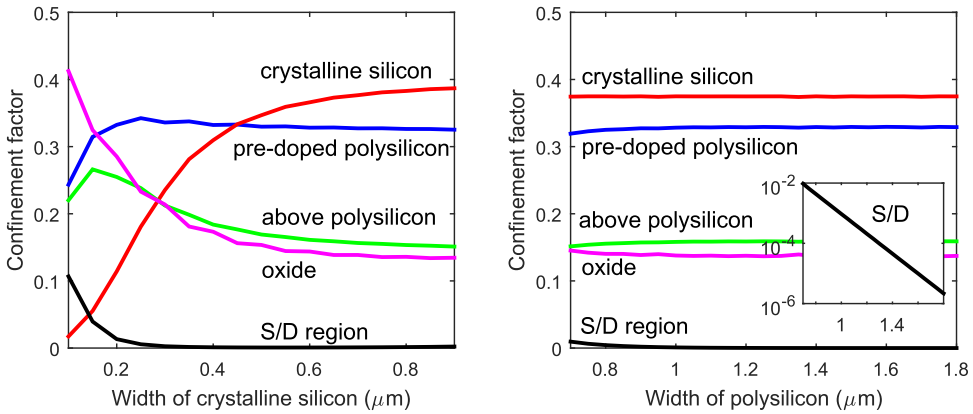

Fig. 3. (a) Crystalline silicon ridge width of 600 nm keep confinement factors in S/D region small Additionally, it also reduce confinement factor above polysilicon. (b) Central polysilicon width of 1.6 μm reduces the confinement in S/D region to below 0.1%.

confinement is almost unchanged in the polysilicon. A body silicon width of 600 nm minimizes the field confinement above the polysilicon and consequently field overlap with polysilicon top surface roughness while maintaining single-mode operation. Figure 2(c) shows the profile of the optical mode of this waveguide. Numerical simulation indicates that the confinement factor in the polysilicon layer is around 0.32 in this device.

In this CMOS process, the polysilicon gate is pre-doped either n-type or p-type prior to the source and drain (S/D) doping. As a result, it is not possible to implement a p-i-n diode in the polysilicon. Nevertheless, despite the n-type pre-doped polysilicon center region in the inverse ridge structure, we implement a lateral p-n junction using the S/D doping masks as shown in Fig. 2(b) to provide a built-in field however small to assist photo-generated carrier collection. We block the center part of the polysilicon that overlaps with the optical mode from the S/D doping to avoid extra free-carrier loss. The width of the center part that is free from S/D doping is 1.6 μm. As shown in Fig. 3(b), the confinement factor in S/D region smaller than 0.1%. The distance between between two metal contacts are 3.6 μm.

In order to reduce device size while maintaining adequate light absorption, a ring resonator structure is used to enhance the optical field. The schematic of the ring resonator photodetector is shown in Fig. 2(d). The ring has a radius of 12 μm and is designed to be critically coupled to maximize optical absorption. This requires the round-trip optical loss to be equal to the cross-couple strength, which is dictated by the gap size between the ring and the bus waveguide. A set of devices with coupling gaps varying between 130 nm and 340 nm are designed based on the expected range of polysilicon loss. An illustration of the coupling region and its mode profile is shown in Figs. 2(e) and 2(f), respectively.

For coupling light into and out of the chip and for general signal routing on the chip, vertical grating couplers and waveguides designed in the low-loss body crystalline silicon layer are employed [7]. A taper in the polysilicon layer is introduced to convert the optical mode between the two regions with low insertion loss. We designed 50 μm long linear tapers with a width starting at 0.76 μm and ending at 3 μm. Our numerical simulation results indicate an insertion

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loss of 0.45 dB for each taper, excluding the material loss from polysilicon.

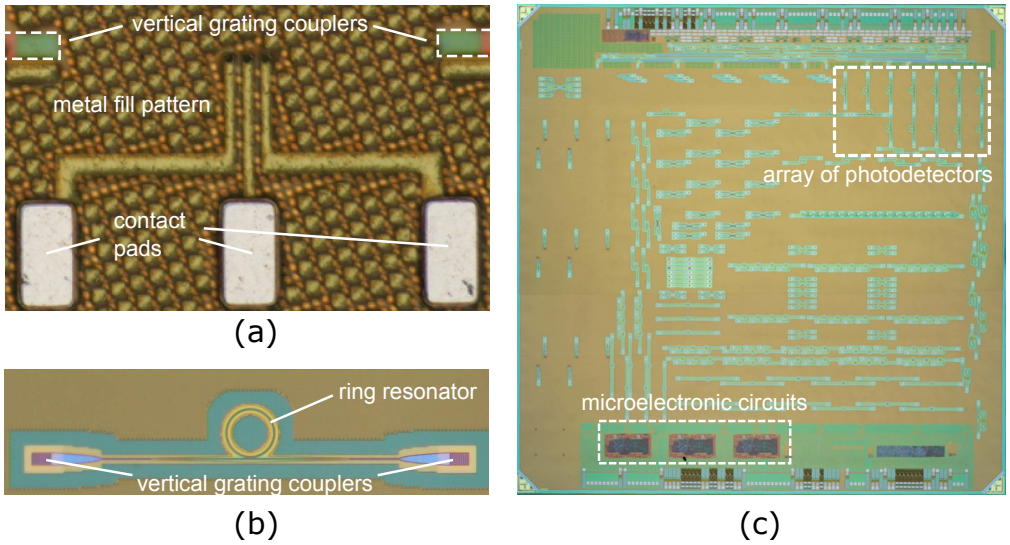

Fig. 4. (a) Photo of the front side of the photodetector. The device is under the fill shapes of the top metal layers that are only blocked from the vertical grating couplers to enable coupling into the chip. The GSG contact pads are connected to the two device terminals through vias and metal interconnect layers. (b) Photo of back side of the device after the silicon substrate is completely removed in a Xenon Difluoride etch chamber. (c) Photo of the back side of the die. Electronic circuits and photonic devices are integrated monolithically.

The photodetectors are fabricated in IBM(now Global Foundries) 45 nm SOI CMOS process. Figure 4(a) shows the optical micrograph of one of the resonant photodetectors with Ground-Signal-Ground (GSG) padset that is connected to the two terminals of the device. The first few metal interconnect layers within 2 μm from top surface of polysilicon are blocked in the design to avoid overlap with the optical mode. The higher metal layers that are far from the optical mode are not blocked except for regions over the input and output vertical grating couplers as seen in Fig. 4(a). Since the thickness of BOX layer on the substrate in this process is not enough to prevent leakage of light into the substrate, device layer with all backend interconnect layers are transferred onto a glass substrate as reported in [7]. Figure 4(b) shows the optical micrograph of the photodetector from the backside through the transparent BOX layer after the release of silicon substrate and before transfer to the glass substrate. Fig. 4(c) shows that the microelectronic circuits and photonic devices are integrated side by side on the same CMOS chip. Previous work [7] shows that the substrate removal does not affect the functionality of electronic circuits.

3. Result and Discussion

The resonance of the ring from 1520 nm to 1580 nm is shown in Fig. 5(a). Extinction more than 10 dB is obtained in the whole wavelength range. The free spectral range (FSR) is around 9 nm. The resonance condition of the ring with different gap sizes between ring and bus waveguides are shown in Fig. 5(b). It can be observed that the photodetector with a gap size of 160 nm has the highest extinction ratio of more than 25 dB. This device has an intrinsic Q factor of 5000

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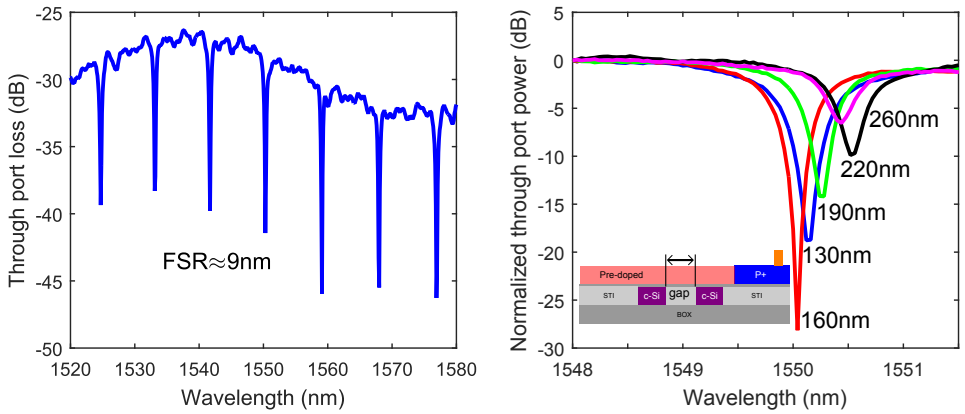

Fig. 5. (a)Resonance is achieved from 1520 nm to 1580 nm. The FSR is around 9 nm. (b)Highest extinction is obtained at gap size of 160 nm. Gap sizes between 130 nm and 190 nm production extinction more than 10 dB.

and loss around 130 dB/cm. Previous work in our group shows a loss of 60 dB/cm for a pure polysilicon strip waveguide in the same CMOS process. The ratio between these two waveguide losses is close to the ratio of their confinement factors (0.32 versus 0.13). This indicates that the polysilicon is dominating the optical loss.

Additionally, it can be observed that for photodetectors with gap sizes in the range of 130 nm to 190 nm the extinction ratio remains above 10 dB corresponding to more than 90% power drop in the resonator. This indicates that the absorbed light in the photodetectors are not sensitive to process variations.

The I-V curves of the photodetector are shown in Fig. 6(a). The blue curve shows the dark current. It can be observed that the dark current rises almost exponentially with voltage in both forward and reverse bias. Additionally, no obvious diode turn-on can be observed. The dark current at 25 V reverse and forward bias is roughly 100 nA and 1 μA, respectively. We attribute the high current level in the reverse bias to carrier tunneling across the p+/n+ junction due to the high doping level in the pre-doped region [reference for tunneling]. Because of the high current tunneling in the reverse bias, our device operates similar to a photoconductor with an asymmetric response.

The red curve in Fig. 6(a) shows the photocurrent as a function of bias voltage for 40 μW of optical power entering the resonant detector. The photocurrent follows a similar I-V behavior as that of the dark current. The ratio between photocurrent and dark current has a maximum of 17.8 dB at 11.75 V bias. The photocurrent dynamic range (defined as $10\log(I_{lit}/\sqrt{2qI_{dark}\Delta f})$) with 1 GHz bandwidth is 28.8 dB at around 18 V forward bias. Additionally, an open circuit voltage of roughly 0.25 V can be observed. This indicates a built-in potential in the photodetector because of the implementation of the p-n junction.

The responsivity is calculated from the photocurrent and optical power reaching the detector. We estimate the optical power in the input fiber using a power tap monitor. The optical power entering the photodetector is calculated from the optical power in the input fiber and the insertion loss from the input grating coupler to the photodetector. This insertion loss is estimated at half of the total insertion loss from the input to output fibers at an off-resonance wavelength.

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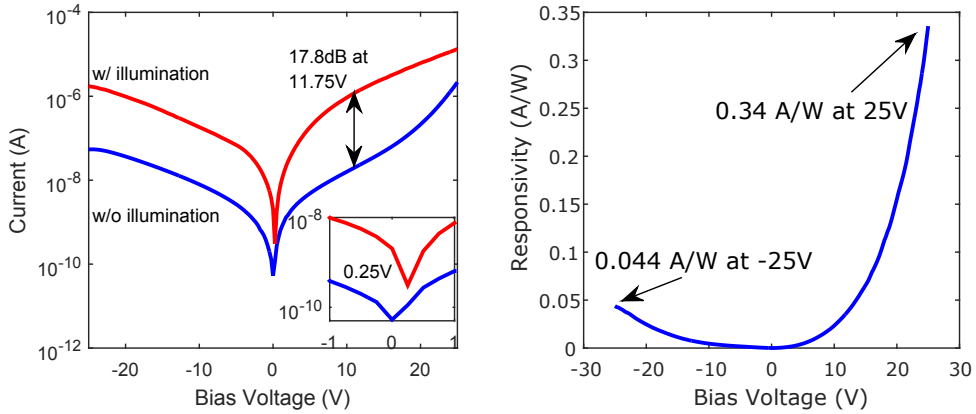

Fig. 6. (a) I-V curves of the resonant photodetector without and with 40 μW light launched into the waveguide. The inset shows a close-up of the I-V curve near the 0 V bias showing an open-circuit voltage. (b) Responsivity at 1550 nm versus bias voltage with 40 μW optical power into the device.

We assume the insertion loss at the input and output to be roughly the same because of identical grating couplers and fiber tilt angles. The calculated responsivity is plotted in Fig. 6(b). The responsivity at 1550 nm is 0.044 A/W and 0.34 A/W at 25 V reverse and forward bias, respectively.

We measured the dependence of the responsivity of the photodetector to input optical power. Figure 7(a) shows the results under 5 V reverse and forward bias conditions for a resonance at 1570 nm. It is observed that the responsivity drops with optical power. It is possible that generation or extraction of carriers are inversely dependent on carrier concentration, as reported in recent literature [26, 27]. Another possible explanation is increased field screening due to more photo-generated carriers at higher power.

We have also measured the responsivity of the resonant photodetector over a wide wavelength range covering E, S, C, and L bands. Figure 7(b) shows the normalized responsivity of the photodetector from 1360 nm to 1630 nm normalized to the responsivity at 1550 nm under 5 V forward bias. It is observed that the responsivity is relatively flat in this wavelength range. This is encouraging as it allows these type of defect-based photodetectors to be used in a wide range of wavelengths that covers telecommunication and data-communication.

Because of the sensitivity of the responsivity to optical power (see Fig. 7(a)), this measurement requires particular attention to assure the optical power is fixed across the measurement wavelength range. Two factors have to be pre-corrected for this purpose: 1) the insertion loss of the input grating coupler that varies by nearly 10 dB over this wavelength range; 2) coupling condition and the Q of the resonances that vary with wavelength. We took these factors into account and pre-corrected the optical power of the laser to assure the optical power of the photodetector resonant mode is 20 μW.

The bandwidth of the photodetector is measured at 15 V forward and reverse bias. The result is shown in Fig. 8. It can be observed that the 3 dB bandwidth is around 1 GHz for both forward and reverse bias. Additionally, a bandwidth measurement was performed at different bias voltages, such as -25 V, -5 V, 10 V and 17.5 V. The measured 3 dB bandwidth are all around

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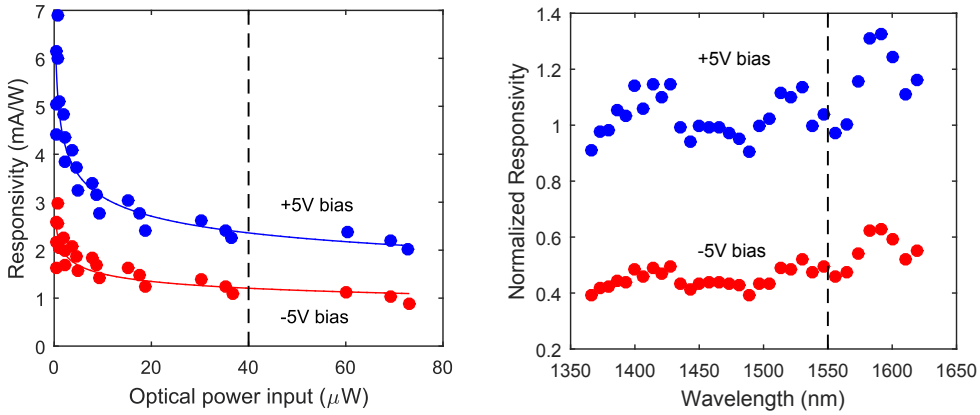

(a) (b)

Fig. 7. (a) Responsivity of the resonant photodetector as a function of the optical power entering the resonator at 1570 nm under 5 V reverse (red curve) and forward (blue curve) bias. (b) Responsivity of the photodetector from 1360 nm to 1630 nm for 20μW optical power entering the resonator normalized to responsivity at 1550 nm with 5 V forward bias.

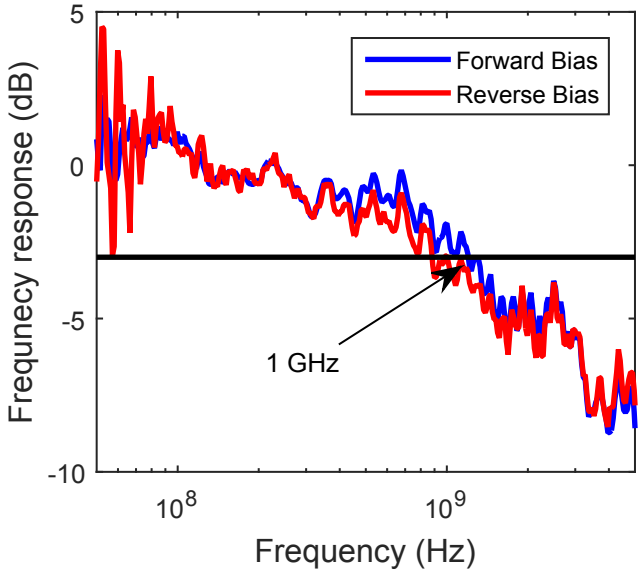

Fig. 8. The 3 dB bandwidth under both forward and reverse bias is around 1 GHz

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1 GHz. In previous work [28], modulators with exactly the same contact pads and vias work at 5 GHz. Therefore, we believe RC limit is unlikely. The limit to bandwidth could be transit time between the two metal contacts, which are 3.6 μm away. It is possible that the carrier saturation velocity in polysilicon is reached when the bias voltage is above 5 V.

4. Conclusion

A guided-wave photodetector based on defect states in the gate polysilicon was demonstrated in zero-change SOI CMOS platform in telecommunication wavelength for the first time. We designed a new inverse ridge structure employing both gate polysilicon and body crystalline silicon layers to minimize unwanted sources of optical loss while providing enough field overlap with the polysilicon layer. A responsivity of 0.34 A/W was achieved under 25 V forward bias with a dark current of around 1.4 μA. The maximum dynamic range measured is 28.8 dB. By implementing balanced detection scheme, the receiver dynamic range can be better than that of the detector [29]. The 3 dB bandwidth of this device is measured to be 1 GHz which is adequate for on-chip power monitoring purposes [6].

We believe that the infrared photodetector demonstrated in this work can be used to implement 1D and 2D photodetector arrays in 1300-1600 nm range that currently does not have a low-cost solution in standard CMOS. Using a microlens array the incident light can be focused onto an array of vertical grating couplers terminated on waveguide-based IR photodetectors. A similar 2D vertical grating coupler array architecture has been demonstrated recently for a LIDAR application [5, 30]. The combination of low-loss waveguide and high-Q resonators on the SOI CMOS platform with the photodetectors demonstrated in this work can enable single-chip infrared spectrometers in a wide wavelength range that can lead to low-cost solutions for applications such as absorption spectroscopy and optical coherence tomography.

The performance of the photodetector can be further improved. The distance between two metal contacts can be reduced to around 1 μm without introducing significant optical loss. If the photoconductor speed is indeed transit-time limited, the 3 dB bandwidth can then be increased to around 3.6 GHz. With small changes in process, the performance can potentially be further improved. If intrinsic polysilicon is available as the absorption region, the free carrier loss will be smaller and the dark current can be reduced significantly. With a chemical mechanical polished (CMP) polysilicon top surface, scattering loss can be reduced significantly as well. Since 3 dB bandwidth of 10 GHz and dark current under 100 pA has been realized using intrinsic CMP polysilicon in a bulk CMOS process [25], it is reasonable to expect this performance can also be realized in the inverse ridge structure presented here, using thin polysilicon and thin crystalline silicon. Additionally, a better responsivity than the current 0.34 A/W should be feasible due to less loss. Such a device has the potential to transform many telecommunication applications.

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