A 45nm SOI Monolithic Photonics Chip-to-Chip Link with Bit-Statistics-Based Resonant Microring Thermal Tuning

Chen Sun[1,2], Mark Wade[3], Michael Georgas[2], Sen Lin[1], Luca Alloatti[2], Benjamin Moss[2], Rajesh Kumar[3], Amir Atabaki[2], Fabio Pavanello[3], Rajeev Ram[2], Miloš Popović[3], Vladimir Stojanović[1]
[1]University of California Berkeley, [2]Massachusetts Institute of Technology, [3]University of Colorado, Boulder
Email: sunchen@mit.edu

Abstract A new thermal tuning circuit for optical ring modulators enables demonstration of an optical chip-to-chip link for the first time with monolithically integrated photonic devices in a commercial 45nm SOI process, without any process changes. The tuning circuit uses independent 1/0 level-tracking and 1/0 bit counting to remain resilient against laser self-heating transients caused by non-DC-balanced transmit data. A 30fJ/bit transmitter and 374fJ/bit receiver with 6μA$_{pk-pk}$ photocurrent sensitivity complete the 5Gb/s link. The thermal tuner consumes 275fJ/bit and achieves a 600 GHz tuning range with a heater tuning efficiency of 3.8μW/GHz.
Keywords: Optical, Link, Ring, Resonator, Thermal Tuning

Silicon photonics is an emerging technology with the potential to overcome traditional I/O limitations. Dense wavelength-division multiplexing (DWDM), in particular, promises order of magnitude bandwidth density improvements, relieving chip-to-chip bandwidth bottlenecks. The key enabler of DWDM is the optical microring, a resonant μm-scale device used for both wavelength-selective modulators and receivers. As a high Q-factor resonant device, however, the ring is sensitive to both process variations and thermal perturbations (10GHz/K temperature drift), necessitating closed-loop thermal tuning to wavelength-lock the resonance to the laser.

In this work, we present a transmit-side thermal tuner that utilizes photocurrent from an integrated drop-port photodetector (PD) and 1-bit, 0-bit counts of the transmitted data to perform power level tracking of transmitted 1s and 0s. This enables correct operation when the 1/0 balance of data fluctuates, avoiding the limitations of averaged power tracking [1, 2]. The integrator is more sensitive than a high-speed sampler used in direct-sampled level-tracking [3], enabling a weaker drop-port tap to preserve resonator Q-factor. We utilize this concept to demonstrate the first monolithically-integrated optical chip-to-chip link in a zero-change 45nm SOI process.

The thermal tuner (Fig. 1) is divided into a frontend and a backend. The frontend integrates drop-port photocurrent for a configurable interval of 16-128 transmitted bits and a SAR ADC converts the integrator output to digital. The backend collects 1/0 counts of the transmitted bits and an aligner FSM coordinates the start/reset times of the integrator and counter to match the integration window with the counted bits. Using the ADC output and 1/0 counts, the solver calculates the power levels of optical 1s and 0s (L_1 and L_0) as well as the modulation depth ($L_{diff} = L_1 - L_0$), i.e. the vertical eye opening.

The tuning controller (Fig. 2) in the backend is an FSM that finds and locks the ring to a lock point that maximizes L_{diff}. The tuning controller operates slower than the heater-to-ring temperature time constant. During the auto-lock procedure, *init* sets the heater DAC setting (P_H) to an initial value $P_{H\text{-}init}$ and *search* steps P_H in large strides until L_0 is less than a set threshold R_{sweep}, indicating coarse alignment of the resonance

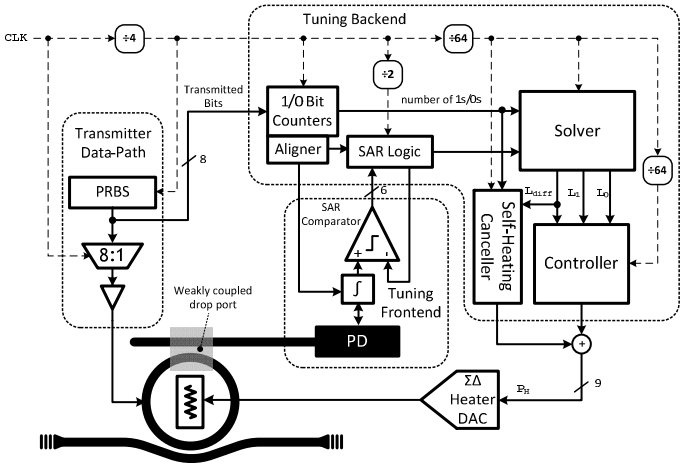

Fig. 1 Transmitter thermal tuner block diagram

to the laser. Next, *sweep* steps P_H by 1 LSB as the controller maps the shape of the resonance, finding $P_{H\text{-}opt}$, $L_{0\text{-}opt}$, and $L_{diff\text{-}opt}$ of the optimal lock point. When L_0 is again > R_{sweep}, the controller exits the *sweep* state. To return back to the optimal lock point, the *reset* and *return* states set P_H=$P_{H\text{-}init}$ before setting P_H=$P_{H\text{-}opt}$, ensuring that the optimal lock point is always approached from the same heating direction and guaranteeing the return to the correct lock point given laser heating-induced resonator bi-stability. The *lock* state maintains the lock under thermal perturbations.

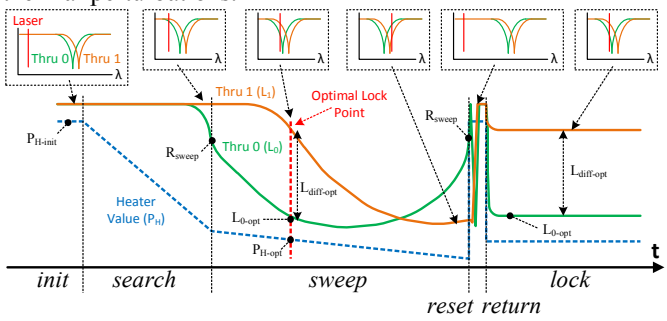

Fig. 2 Tuning controller lock-on waveform with the transfer function of the ring shown with respect to the laser position at each state

The self-heating canceller mitigates sudden changes in ring-absorbed optical power (resonating laser power) from a change in 1/0 balance, which disrupts the resonance before the controller can react. The canceller uses 1/0 counts and L_{diff} to provide an adequate change in P_H to null changes in self-heating power.

We incorporate the thermal tuner as part of the monolithically-integrated 45nm SOI photonics transceiver platform (Fig. 3) with re-optimized circuits from [4]. The modulator driver is an inverter chain which drives the modulator device cathode, providing a swing of V_{DD} across the device. The modulator anode connects to V_{BIAS}, allowing adjustment of the swing offset. The receiver consists of a SiGe PD connected to a TIA, followed by two sense-amplifier

comparators operating on opposite clock phases. The low parasitic capacitance afforded by monolithic integration enables high-bandwidth and sensitivity from a single-stage inverter TIA design with a feedback resistance of 5kΩ. Capacitive and current DACs in the comparator and TIA input allow for adjustment of the receiver decision threshold, providing offset compensation and eye-monitoring.

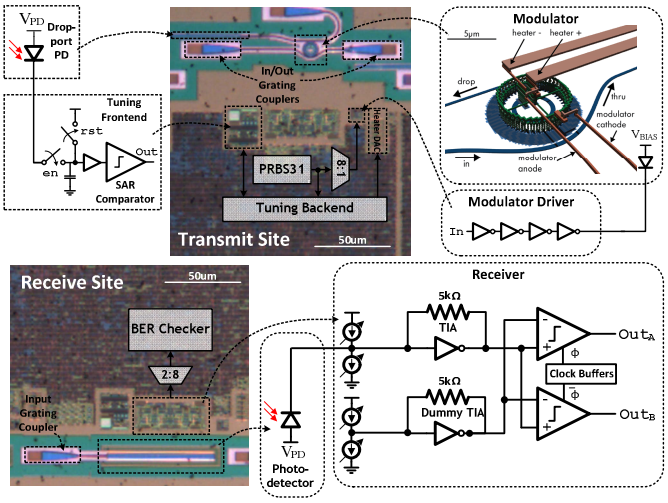

Fig. 3 Tuning transceiver implementation in 45nm SOI

The tuning circuitry auto-locks the modulator ring (with a non-heated resonance at ~1187.2nm) to a non-tunable 1189nm laser, finding the lock point that maximizes L_{diff}. A PRBS31 sequence is used for both the lock-on process and eye-measurement (Fig. 4). Under a swing of -0.7V to +0.5V (V_{DD} = 1.2V, V_{BIAS} = +0.5V) at 5Gbps, we achieve a 6.5dB extinction ratio (ER) at an insertion loss (IL) of 4dB. With forward-biased voltages, electrical junction characteristics limit the data-rate to 5Gbps. An open modulator eye can be maintained up to 8Gbps using fully reverse-biased swings (-1.2V to 0V), though ER degrades to 2.3 dB. The driver energy cost is 30fJ/bit with V_{DD} = 1.2V for all data rates.

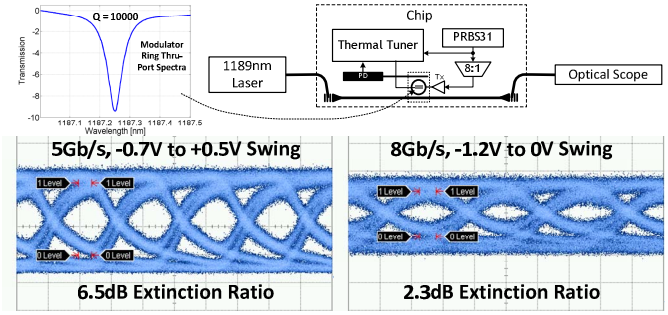

Fig. 4 Transmitter auto-locked using the thermal tuner

We use a controller decision rate of 76KHz (2 controller clock cycles at 5Gbps). The upper-bound on lock time is 7ms, assuming a 1 LSB step size for *search* and a worst-case $P_{H\text{-}init}$ from the final lock position. The tuner frontend sensitivity is <500nA, though the drop-port PD provides ~3.5 µA of current for the laser power used. The frontend (integrator, SAR ADC) and backend consume 39fJ/bit and 236fJ/bit, respectively. De-embedding from simulation, we note that 80% of the backend power comes from the synchronous 1/0 bit counter, the aligner, and their clock buffers (all on the least divided clock), which were synthesized for a much higher frequency than intended. The ΣΔ heater driver DAC provides 600GHz (3nm) of tuning range (~60K of temperature change) and delivers 3.8µW/GHz overall tuning efficiency.

To demonstrate the full capabilities of the level-tracking circuitry and the self-heating canceller, we randomly change the 1/0 balance (uniform distribution) of the transmitted data every 200ms (Fig. 5), including the all 0s and all 1s cases. With the tuning circuit operating in average power lock mode (tracking average photocurrent only), the modulator eye is completely closed as the controller is unable to discern a change in 1/0 balance from a drift in resonance. Independent 1/0 level tracking allows the controller to lock correctly. However, the sudden change in heating from the laser when the 1/0 balance changes causes transient eye closure until the controller can react. When enabled, the self-heating canceller compensates for this effect, allowing the eye to remain open.

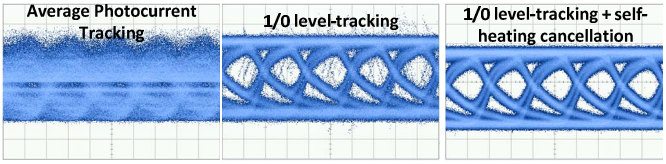

Fig. 5 Tuning experiment with randomly changing 1/0 balance in the transmitted data. All eyes are 5Gb/s, taken for a full minute.

We demonstrate the full functionality of the transmitter, receiver, and thermal tuner in a chip-to-chip optical link at 5Gb/s with $<10^{-10}$ BER (Fig. 6). At 5Gb/s, the receiver circuit (Rx) achieves 6µ$A_{pk\text{-}pk}$ sensitivity at 374fJ/bit. Though there are PDs on this chip that demonstrate >0.1A/W responsivity, they are not connected to the tested receiver circuits. To overcome the limited responsivity of the PD of the tested site (0.02A/W), we insert an optical amplifier between the two chips. We note that the amplifier adds 7.5 dB of gain to the peak-to-peak signal, but also degrades extinction ratio due to non-linear gain and broad spectrum power output.

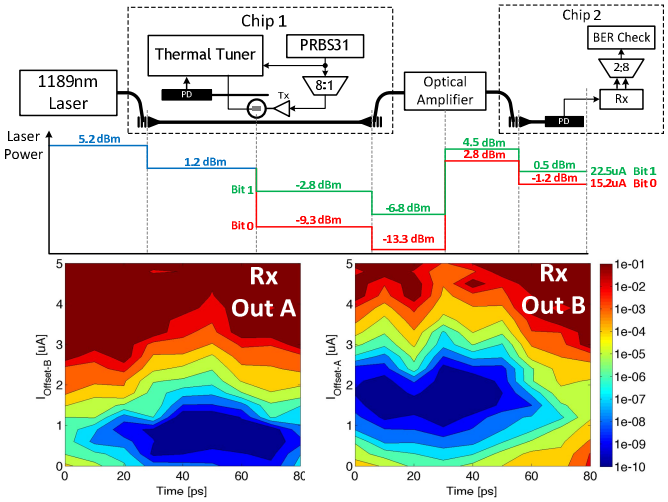

Fig 6 Chip-to-chip link demo with optical power labeled at each stage

This work demonstrates 1/0 optical level tracking, self-heating cancellation, and modulation depth optimization as essential techniques for tuning resonant microrings, enabling a robust link platform for chip-to-chip I/O.

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