Depletion-mode carrier-plasma optical modulator in zero-change advanced CMOS

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We demonstrate the first (to the best of our knowledge) depletion-mode carrier-plasma optical modulator fabricated in a standard advanced complementary metal–oxide-semiconductor (CMOS) logic process (45 nm node SOI CMOS) with no process modifications. The zero-change CMOS photonics approach enables this device to be monolithically integrated into state-of-the-art microprocessors and advanced electronics. Because these processes support lateral *p-n* junctions but not efficient ridge waveguides, we accommodate these constraints with a new type of resonant modulator. It is based on a hybrid microring/disk cavity formed entirely in the sub-90 nm thick monocrystalline silicon transistor body layer. Electrical contact of both polarities is made along the inner radius of the multimode ring cavity via an array of silicon spokes. The spokes connect to *p* and *n* regions formed using transistor well implants, which form radially extending lateral junctions that provide index modulation. We show 5 Gbps data modulation at 1265 nm wavelength with 5.2 dB extinction ratio and an estimated 40 fJ/bit energy consumption. Broad thermal tuning is demonstrated across 3.2 THz (18 nm) with an efficiency of 291 GHz/mW. A single postprocessing step to remove the silicon handle wafer was necessary to support low-loss optical confinement in the device layer. This modulator is an important step toward monolithically integrated CMOS photonic interconnects.

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To enable the continued scaling of massively multicore processors and the realization of the exascale supercomputing paradigm, processor-to-memory interconnect power consumption must be dramatically reduced while data bandwidth density is increased. Wavelength-division-multiplexed (WDM) optical interconnects are emerging as the most promising technology to replace electrical CPU-DRAM interconnects [1]. Substantial progress has recently been made in the development of optical interconnects based on photonic components monolithically integrated with state-of-the-art microelectronics using no process changes [2].

In this Letter, we demonstrate a depletion-mode modulator in a commercial CMOS foundry running a standard 45 nm process (IBM 12SOI [3]). No modifications to the process flow were allowed by the foundry nor were required by the design. To accomplish this, a novel modulator structure was devised. A single postprocessing step to remove the silicon substrate was necessary to provide complete optical confinement, and was shown previously to have no effect on the performance of electronics on chip [2]. The modulator occupies 80 μm^2 in area and was demonstrated at 5 Gbps, with 5.2 dB extinction ratio and an estimated energy consumption of 40 fJ/bit.

This result represents a significant step toward the realization of full photonic links and interfaces in advanced CMOS electronics, because it demonstrates energy-efficient, depletion-mode optical modulators that are fully compatible with a native CMOS process flow. This approach eliminates the need for hybrid integration [4], modifications to existing CMOS processes, or even additional lithographic masks. Previously demonstrated devices that were described as CMOS compatible depend on a thick silicon device layer with partial etch steps [5–7], vertical junctions [8] (ill-suited for implementation in a thin transistor device layer), or specific implantation conditions not common to transistors—none of which are available in a state-of-the-art CMOS process used for microprocessors.

Instead of a ridge waveguide, we use a multimode ring cavity formed in the fully etched transistor body silicon layer. Optical mode confinement is provided by the outer-radius step-index boundary of the cavity, while

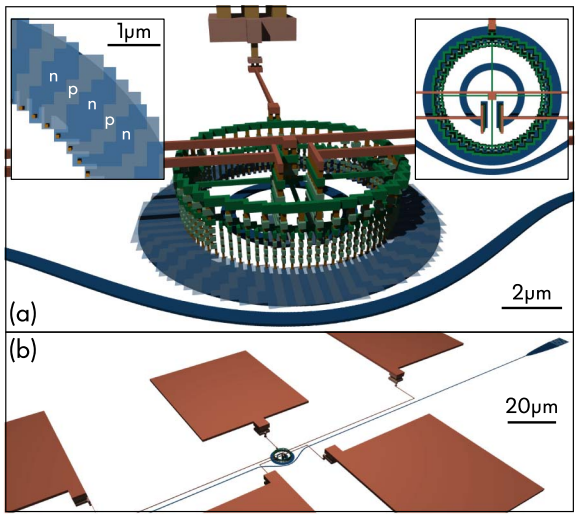

Fig. 1. (a) Layout of monolithically integrated modulator showing spoked contacts, radial *p-n* junctions, mode-selective waveguide coupler, and back-end metal stackup (left inset, contacts and lateral junctions; right inset, top view showing central heater). (b) Zoom-out: driver and heater contact pads and input grating coupler.

all electrical contacts are placed along the inner-radius boundary of the cavity. Lateral *p-n* junctions—for index modulation—are formed from implants present in the transistor process.

The design is shown in Fig. 1, including the device layer, implant masks, and several layers of electrical connections including vias and metals. We utilize disk-like whispering-gallery modes of a microring of multimodal width formed in the sub-90 nm thick transistor body device layer of the SOI CMOS process (exact layer dimensions available in IBM 12SOI Process Design Kit under nondisclosure agreement [3]). Eighty-four lateral *p-n* junctions extend radially out and are azimuthally distributed around the ring [left inset of Fig. 1(a)]. The ring cavity is wider than the single-mode width to allow electrical contacts placed at the inner-radius edge to impart minimal optical loss to the fundamental mode. Although the higher-order spatial modes are suppressed in Q by scattering from these contacts and bending loss, they remain high enough Q to have an undesirable spectral signature. Hence, excitation of only the fundamental mode, and suppression of the higher-order modes, is further accomplished by a suitably designed coupler. A propagation-constant-matched, curved bus-to-resonator coupler with a long interaction length has a small k-space spread of the perturbation and does not excite the higher-order, low-Q resonances [9,10]. The 5 μm outer ring radius is larger than the minimum permitted by bending loss to accommodate an efficient coupler design.

The optical transmission spectrum in Fig. 2(a) shows that only the fundamental family of (TE-polarized) modes is excited in the cavity, as designed. The measured free spectral range (FSR) is 17 nm near 1260 nm (3.2 THz near 240 THz), and the 3 dB linewidth is 26 GHz near critical coupling, indicating an intrinsic Q of 18,000. Through-port optical extinction exceeds 10 dB near the design wavelength, while overcoupling limits extinction at longer wavelengths. TM-polarized guided modes are not supported in waveguides this thin.

Lightly doped *p-n* junctions are critical to achieving low optical loss and sufficient wavelength shift under drive to effect high-extinction-ratio modulation. The source/drain implants for field-effect transistors in this process cannot be utilized because they lead to dopant concentrations exceeding $10^{19}/\mathrm{cm}^3$, whereas concentrations between $5\times10^{17}/\mathrm{cm}^3$ and $5\times10^{18}/\mathrm{cm}^3$ are more suitable for depletion-mode modulators. We found suitable doping concentrations in well implant [11] modules. The I-V curve [Fig. 2(b)] confirms rectification, and spectral shifts for several DC bias conditions are shown in Fig. 2(c). Tuning of 17 pm/V is achieved.

To maximize the optical wavelength shift for a given voltage swing, the angular width of each spoke should be chosen so that, in the maximally reverse-biased state, each spoke unit cell (hence the entire cavity) is nearly fully depleted of carriers. For the dopant concentrations considered here, this would require 140 nm wide regions of each dopant. However, design rules for implant mask layers limit this width to ~220 nm, and therefore mode shifts are limited to about 60% of what could, in principle, be achieved with these carrier concentrations. Figure 2(c) shows that the mode shifts are sufficiently large to allow for modulation with a modest voltage

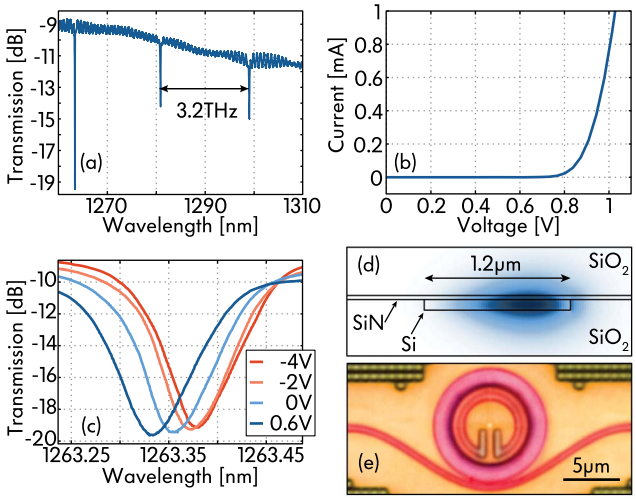

Fig. 2. (a) Optical transmission spectral response with single transverse-mode operation evident (FSR = 3.2 THz, extinction near 1260 nm is >10 dB), (b) device I-V curve, (c) resonant optical response at DC bias voltages from −4 to +0.6 V, (d) calculated cross-sectional mode profile (the waveguiding body silicon and the nitride liner layer above it are outlined), and (e) optical micrograph of the device taken from below after removal of the handle Si wafer.

swing. For optical excitation at 1263.33 nm, at the bottom of the resonant dip at +0.6 V applied bias, we expect near 6 dB modulation depth when switching to a reverse bias between −2 and −4 V.

Figure 3(a) shows an eye diagram acquired on a sampling oscilloscope with a 10 GHz optical sampling module and 5 GHz low-pass filter. The device was driven with a 5 Gbps, 2^7-1 bit pseudo-random binary sequence, by a 40 GHz GSG probe. Longer bit patterns were not investigated due to drift in the optical alignment. The GSG probe pad and wiring layout is shown in Fig. 1(b). Due to impedance mismatch between the 50 Ω driving probe and the device, voltage doubling is expected at the device, and the voltage swing actually seen by the modulator is −3 to +0.6 V—a range accessible to integrated driver circuits. Under these operating conditions, 5.2 dB modulation depth was measured with 4.5 dB insertion loss, consistent with DC mode shifts shown in Fig. 2(c). The average switching energy ($(1/2)CV_{pp}^2$ for NRZ data) is estimated from the voltage swing and a computed device capacitance (12 fF) to be 40 fJ/bit. The maximum leakage current measured in any tested device was 16 μA at 0.6 V; this places an upper limit of 1.2 fJ/bit on the energy consumption due to driving current. To one significant figure, the total energy consumption of the device under these driving conditions is estimated to be 40 fJ/bit. This is comparable to state-of-the-art custom-process devices [4].

Scaling the cavity size does not impact speed but does affect energy efficiency. The RC time constant of the array is equal to that of a single spoke, and therefore the device speed is independent of the number of spokes and thus independent of the ring radius. The optical Q is also independent of radius to first order, so neither electrical nor optical bandwidth is governed by the cavity size. However, the device energy is proportional to total device capacitance and thus to radius. Also, the device

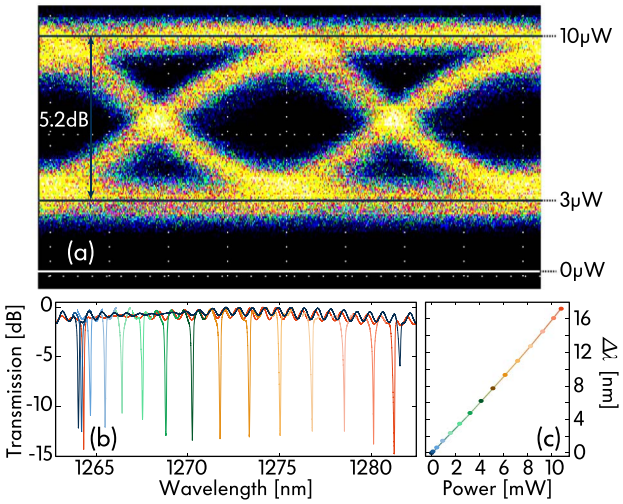

Fig. 3. (a) 5 Gbps optical eye diagram with 5.2 dB modulation depth in response to drive voltage swing from −3 to +0.6 V (at the device terminals), (b) thermal tuning of the modulated resonance across a full FSR (efficiency: 291 GHz/mW), and (c) linear resonance tuning versus heater power.

can rely on single-boundary (outer-radius) optical confinement to produce a small transverse mode, and small series resistance, only at smaller radii.

In a WDM transmitter, modulators are multiplexed along a waveguide, each tuned to a wavelength channel. For active wavelength tuning, a resistive microheater was included in the modulator cavity [Fig. 1(a), inset]. The heater is also formed in the body silicon layer and employs the process source/drain implants to give a 10 kΩ resistance. While tuning on the order of a channel spacing (~1 nm) is required, Fig. 3(b) shows tuning of a full FSR with an efficiency of 1.6 nm/mW (291 GHz/mW). At 5 Gbps, this corresponds to 125 fJ/bit/nm.

We expect higher speed, greater modulation depth, lower insertion loss, and higher energy efficiency to be achievable with modest modifications to this design. The optical cavity design in this work was conservative to ensure high enough optical Q amid process uncertainties. In future designs, a narrower ring width and contacts placed closer to the optical mode will reduce both resistance and capacitance. Changes of a few hundred nanometers could more than double the cutoff frequency and significantly reduce the energy consumption per bit by reducing the capacitance. Greater modulation depth and reduced insertion loss can be achieved by reducing the width of the spokes by almost a factor of two, but in the current process this would require a design rule waiver. Finally, the devices were designed with radially extending junctions, but were implemented with zig–zag approximations to this geometry [left inset of Fig. 1(a)] due to a design rule requiring dopants to be laid out on a coarse Manhattan grid. The impact of these geometrical restrictions remains a subject for future study.

We believe that this demonstration of a depletion-mode optical modulator in a commercial 45 nm CMOS logic process, with no modifications required within the foundry, is a watershed milestone toward enabling complete optical links monolithically integrated with advanced CMOS electronics, and implemented directly in existing advanced-node CMOS foundries.

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