Silicon Platform With Vertically Aligned Carbon Nanotubes for Enhancing Thermal Conduction in Hybrid Optoelectronic Integration

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***Abstract*— Silicon platforms with high-number-density vertically aligned carbon nanotubes (VACNTs) on patterned substrates are designed and fabricated to provide efficient thermal conduction for hybrid optoelectronic integration and device packaging. The simulation shows that the platform can reduce the thermal resistance by >40%, resulting from the help of the high-thermal-conductivity VACNTs and the increase in the heat spreading area of the patterned platform geometry. The platform can also provide the flexibility in device attachment and alignment. Applications of this platform to packaged light-emitting diodes (LEDs) are used to demonstrate the feasibility of this approach. The experimental results verify that an increase in the saturation power and optical output power of LEDs can be obtained by packaging with the VACNT-integrated platform. The thermal resistance measurement also indicates that the proposed platform has lower thermal resistance than the planar silicon substrate.**

***Index Terms*— Light-emitting diode (LED), optoelectronic integration, thermal conduction, vertically aligned carbon nanotube (VACNT).**

I. Introduction

SILICON substrates have been the platforms for optoelectronic device packaging due to their thermal and electrical properties [1]–[3]. They are also the popular platforms for heterogeneous photonic circuit integration because of the increased microsystem functionality through integration with other electronic or photonic circuits [4], [5]. Heat conduction of the platform is of critical concern when it is applied to integrate active devices like high-power diode lasers and high-brightness light-emitting diodes (LEDs) [6]–[9]. Poor heat dissipation will result in lower efficiency, shorter lifetime, and wavelength drift for the active devices. Heat conduction is also important for some micro pillar or nanophotonic devices that have larger thermal resistance due to their device geometry [3]. Taking the packaging of high-brightness LEDs as a specific example, silicon substrates are frequently used to replace the original substrates of LEDs due to their good thermal conductivity and relatively low thermal expansion [2]. However, further reduction in the thermal resistance is still strongly desired due to the everlasting efforts of obtaining increasing output power and luminous efficacy for LEDs.

Carbon nanotubes (CNTs) are well-known excellent heat spreaders for their high thermal conductivity and good mechanical strength [10], [11]. They were used as thermal interface material between a LED module and heat sink [12], [13]. They were also used for flip-chip packaging LED chips directly on the CNT-metal electrodes over a silicon carrier [14]. However, the existing ways of using CNTs as heat spreaders usually have poor adhesion between CNTs and adjacent materials, which may impact device yield and reliability. Moreover, heat transfer can be more efficient by placing CNTs closer to heating sources.

In this paper, we designed and fabricated a platform for optoelectronic device packaging by integrating vertically aligned CNTs (VACNTs) onto patterned silicon U-grooves for achieving enhanced thermal conduction and stable mechanical properties. The VACNT structure was demonstrated to have higher thermal conductivity than random CNTs [15], [16]. We applied the platform for packaging LED devices to demonstrate the feasibility of the proposed approach. The enhanced thermal conduction from the use of the platform can be verified from the increased saturation current and output power of the LEDs as well as from the thermal resistance measurement.

II. Design of VACNT-on-Silicon (VoS) Platform

Fig. 1(a) shows the schematic of the platform. VACNTs are grown on a silicon trench to provide heat spreading for the bonded device chip. A thin dielectric layer between VACNTs and silicon substrate is usually needed to eliminate

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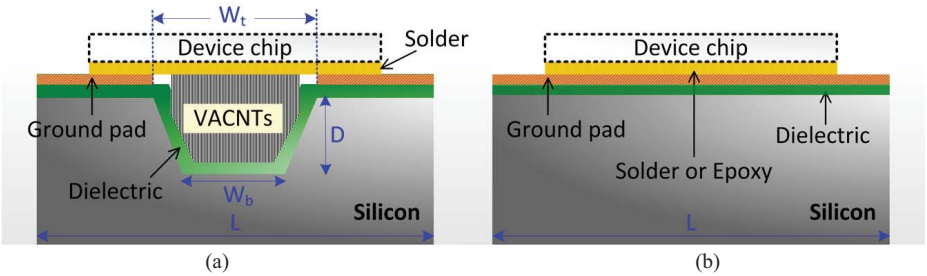


Fig. 1. Cross-sectional view of LED packaging on (a) VoS platform and (b) reference silicon platform.

TABLE I
PARAMETERS FOR NUMERICAL THERMAL MODELING

Component	Thermal conductivity (W/mK)		Dimensions ($L \times W \times T$) (mm^3)
LED substrate	Si	148	$0.3 \times 0.3 \times 0.2$
Submount	Silicon	148	$1.6 \times 0.9 \times 0.2$
	SiO	1.5	
	Silver epoxy	0.68	
	AuSn	60	
	CNTs	150–600	
Heat source has a heat flux of 0.8 W. Bottom boundary: perfect heat conductor with a heat transfer coefficient of 150 000 W/m^2K. Surrounding boundary: static air with a heat transfer coefficient of 220 W/m^2K.			

current leakage to the substrate. The device chip is bonded to the platform by the bonding pads on the platform surface, which provides firm adhesion for the chip to the platform. Since CNTs were known to have larger thermal conductivity than silicon [10], a larger volume of CNTs embedded in the platform leads to a lower thermal resistance for the platform. For comparison, a reference silicon platform with the same thin dielectric layer on top is shown in Fig. 1(b).

The platform can provide not only the enhancement on thermal conduction but also the flexibility in device attachment and alignment. Owing to their mechanical flexibility, the CNTs do not need to have precise length as long as they can touch the bottom of the device chip. This platform can accommodate devices with nonplanar surface, which occurs often in heterogeneous photonic circuit integration. For example, for devices with p-type and n-type contacts on the same side but with different heights, it would be difficult to flip-chip bond the device on planar silicon substrate to obtain good thermal and electric conduction to both contact areas. The bendability also provides flexibility for vertical alignment of the device chip. For example, when the platform is used in combination with the silicon optical bench for packaging a ridge waveguide laser with a fiber [1], the laser can be flip-chip bonded to retain good vertical alignment to the fiber, in addition to the good thermal conduction provided by the CNTs.

The temperature distributions and thermal resistance of the VoS platform were simulated by using the finite element analysis. A silicon monoxide (SiO) film of 500-nm thickness is used as the dielectric layer. The thermal conductivity of CNTs is varied from 150 to 600 W/mK. For the thermal modeling assumption, the boundary environment on the bottom of submount is a perfect heat conductor with a heat transfer coefficient of 150 000 W/m^2K and an area of 1.44 mm^2 (same as the size of submount) for heat dissipation. The boundary surrounding the chip/submount is static air with no forced air flow. The volume heat source is on the surface of device chip with a heat flux of 0.8 W. Thermal resistance is defined as the ratio of the temperature difference between LED junction and surface mounted device (SMD) leadframe over the heat flux. The temperature for the LED junction is extracted from the average value of the top surface while the temperature for SMD leadframe is from the average value of the bottom substrate. The thermal conductivities and device dimensions used in the simulation are listed in Table I. Although the heat transfer coefficient changes with the temperature, the calculated thermal resistance through convection (>3000 K/W) is much larger than that of LED and submount (<15 K/W). It reveals that the dominant heat transfer is through the substrate and the temperature dependence of the natural convective heat transfer only results in minor perturbations to the simulation.

The simulated thermal resistance for the platform is depicted in Fig. 2. The depth ratio for the VoS platform is defined as the ratio of the depth of the U-groove where CNTs reside over the thickness of the substrate. The reference silicon platform with the same thickness of SiO, as shown in Fig. 1(b), is also simulated for comparisons. The heat source has an area of 300 $\mu m^2 \times 300$ μm^2. The VoS platform and the reference silicon platform have the same dimensions of 1.6 mm (length), 0.9 mm (width), and 200 μm (thickness). Fig. 2(a) shows the variation of the thermal resistance with the CNT area ratio, which is the ratio of the top area of the U-groove, W_t^2, over the area of the heat source. The slope of the U-groove was determined by the wet chemical etching (54.75°). The simulated thermal resistance is normalized to that of the reference platform (12.9 K/W). The results indicate that $>40\%$ reduction in thermal resistance can be achieved with an area ratio of 0.8 and a CNT thermal conductivity of 300 W/mK, which is obtainable for single- and multiwall CNTs [10], [11]. The enhancement on the thermal conduction by the VoS platform results not only from the replacement of a portion of silicon substrate with high-thermal-conductivity VACNTs but also from the increased heat spreading due to the platform geometry. The VoS platform increases the surface area of the SiO layer, thereby reducing the thermal resistance. Fig. 2(b) shows that the reduction in thermal resistance can

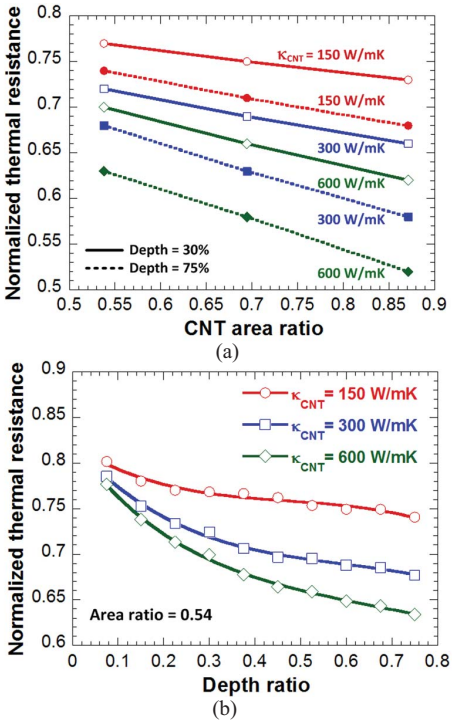


Fig. 2. Simulated thermal resistance versus (a) CNT area ratio and (b) depth ratio for the VoS platform.

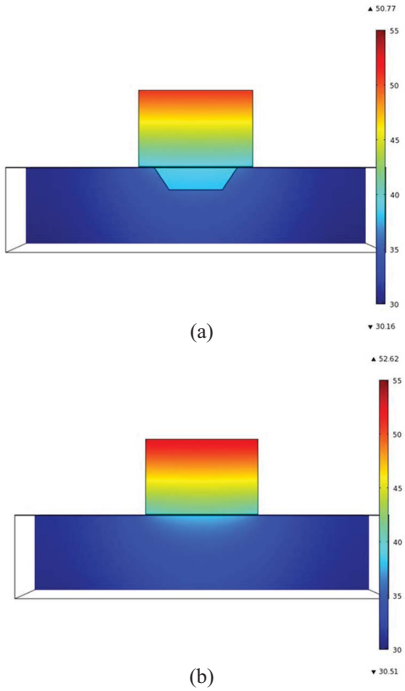


Fig. 3. Simulated temperature distribution for devices packaged on (a) VoS and (b) planar silicon platforms.

be enhanced by increasing the depth of the U-groove and the height of VACNTs, especially for using high-thermal-conductivity CNTs.

Fig. 3 compares the temperature distribution for the device packaging with and without using the VoS platform. In the simulation, the LED chip size is 300 μm^3 $\times$ 300 μm$^3\times$ 200 μm^3 with a thin layer of heat source on the top surface.

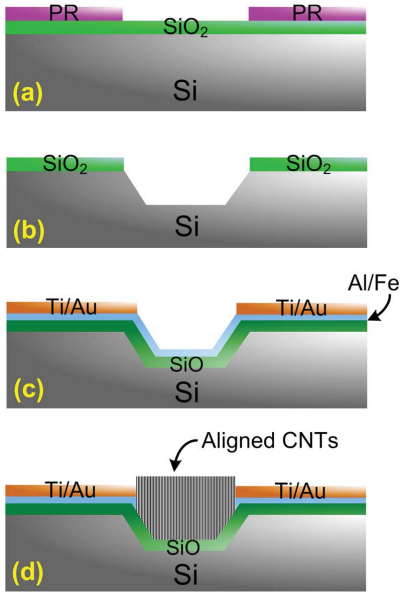


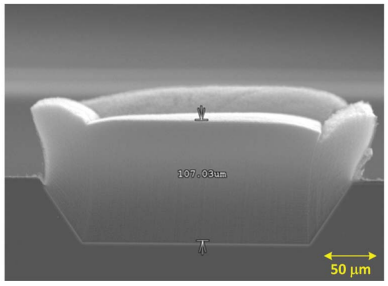
Fig. 4. Fig. 4. Process flow of the proposed LED packaging configuration: (a) deposition of silicon dioxide mask, (b) etching of silicon U-groove, (c) deposition of SiO, Al/Fe, and patterning Ti/Au, and (d) growth of VACNTs.

The substrate of the LED chip is assumed to be silicon. Two-micrometer-thick Au–Sn solder is applied between the LED and CNTs for chip bonding. The thermal conductivity of Au–Sn is assumed to be 60.0 W/mK in the simulation. The heat source dissipates 0.8 W, and the ambient temperature is assumed to be 25 °C. It can be clearly seen from the temperature distribution that the VoS platform can provide excellent heat conduction with the help of heat spreading by the CNT. The heat is effectively conducted by VACNTs to the U-groove sidewalls, which have a larger surface area than the planar silicon surface.

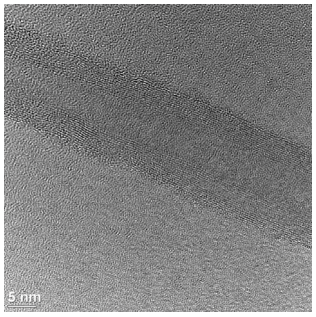
III. Fabrication of VoS Platform

The VoS platform can be easily fabricated with the procedures shown in Fig. 4. Silicon dioxide is first deposited on the 200-μm-thick silicon substrate. After transferring U-groove patterns into silicon dioxide by photolithography and CF_4 plasma etching, the sample is immersed into potassium hydroxide solution with a temperature of 80 °C for 50 min to etch silicon. The opening area and the depth of U-groove are around 210 μm^2 $\times$ 215 μm^2 and 60 μm, respectively. The wet etching condition is optimized for obtaining smooth U-groove surface. A 500-nm-thick SiO film is then deposited over the entire submount for isolating the current from flowing through the substrate.

The VACNT growth is carried out by using the thermal chemical vapor deposition (TCVD) with an Al (5 nm)/Fe (3 nm) thin film as the buffer layer and catalyst, which is deposited over the entire submount. Patterned Ti (50 nm)/Au (500 nm) metal pads are then deposited as the mask for blocking the growth of VACNTs outside the U-groove area and also serving as the ground electrodes. The TCVD growth is performed by first annealing the sample at an elevated temperature of 750 °C and a pressure of 4 $\times$ 10^{-2} torr for 60 min and then pouring in C_2H_2 for 7 min. The SEM photo



(a)



(b)

Fig. 5. (a) SEM photo for the grown CNTs on the U-groove. (b) TEM photo of a single CNT.

shown in Fig. 5(a) indicates that VACNTs with high wire density (around 10^9 wires per square millimeter) can be grown on the U-groove. The CNTs are multiwalled with a diameter of around 16 nm from the TEM photos, as shown in Fig. 5(b).

IV. Applications to LED Packaging

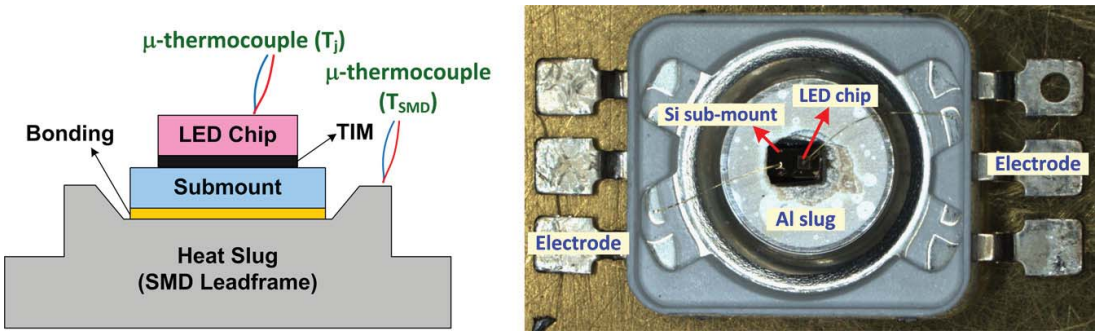
To demonstrate the enhanced heat conduction with the VoS platform, red-emitting LED chips of 300 μm^2 $\times$ 300 μm^2 size are bonded onto the VoS platforms by using Au–Sn solder. The LED chips are top-emitting with a substrate thickness of 200 μm. The assembly is then bonded onto an aluminum heat slug and a SMD leadframe, as illustrated in Fig. 6(a). The Al heat slug has a surface area of 12.56 mm^2 and a thickness of 1 mm. For reference, LED chips were also directly bonded to planar silicon substrates (with thin SiO layer) and then attached to the heat slugs and lead frames. Two types of bonding materials, Au–Sn solder or silver epoxy, are used for the reference samples. There exist fluctuations in the light output characteristics of the LED chips before packaging. In order to make fair comparisons of the LED performance after packaging, tens of samples were packaged on each type of platform. The statistical analysis of the LED characteristics is shown in Fig. 7.

Since the VACNT arrays are grown only inside the U-groove, the LED chips can be firmly bonded to the submount to overcome the adhesion issue between VACNTs and silicon substrate [9]. The bonding quality between LED chips and submounts can be maintained as long as an appropriate planar surface area on the VoS platform is allocated for bonding. In our experiments, the VACNT area is only 54% of that of the LED chip for achieving high packaging yield. The area ratio of the VACNTs can be further optimized to obtain both good thermal conduction and bonding strength.

The light–current–voltage (L–I–V) characteristics are measured by applying a pulse current of 4 s on-time and 3 s off-time on a stage without heat sink. The optical power was measured with a photodetector attached to an integrating sphere. Fig. 7(a) compares the results of the packaged LEDs on different submounts, including the VoS platform, Si substrate with Au–Sn solder, and Si substrate with silver epoxy. The optical spectra shown in the inlet indicate that the light emission has a peak wavelength of 626 nm. The variation of the packaged LED characteristics is partially due to the performance variation of original LED chips. The average saturation current and maximum output power for the silver epoxy packaged LEDs are around 120 mA and 26 mW, respectively. For Au–Sn packaged LEDs, the average saturation current and maximum output power are around 160 mA and 28 mW, respectively. The LEDs packaged with the VoS platform can provide an average maximum output power of around 29 mW and an average saturation current of 170 mA. It can be clearly seen that the LEDs packaged with epoxy bonding have lower output power. Though the performance of the other two packaging types is close, the LEDs packaged on the VoS Platform have better performance than the LEDs packaged with planar silicon substrate, in terms of the average output power. It will be shown later that the thermal resistance difference is small between the LEDs packaged on the VoS platforms and planar substrates with Au–Sn bonding. The resultant temperature difference is thus small since the power consumption of the LEDs is only 0.8 W.

Since the optical output power is only a small portion of the injected electric power, the thermal heating effect can be observed from the analysis of the saturation current. For the LED packaging on planar silicon substrate with silver epoxy, all samples have lower than 120 mA of saturation current. This can be attributed to the low thermal conductivity of silver epoxy. The enhanced thermal conduction by using CNTs can be verified by comparing the saturation current between the packaged LEDs on the VoS platform and planar silicon substrate with Au–Sn solder. Fig. 7(b) shows the histogram of the saturation current for both type of packages. The saturation current values are extracted at the roll-off points of light–current curves of all the devices shown in Fig. 7(a). 55% of the VoS-packaged LEDs have a saturation current equal to or larger than 160 mA, compared to 26% for the LEDs packaged on planar silicon substrate.

To verify the improvement on thermal conduction by VACNTs, the LED junction temperature and leadframe temperature were measured by using microthermocouples, as indicated in Fig. 6(a), which have a temperature resolution of 0.01 K and a data deviation of around 0.1 K [17]. The LEDs are biased at 250 mA to enhance the thermal heating effects. Current/voltage source has a voltage fluctuation of $<$10 μV and a current fluctuation of $<$1 μA. Device dimensions are obtained from the Hitachi scanning electron microscope which has a resolution of 10 nm at 3 kV. During measurements, the sample is attached to a large heat sink. The sample is covered to block the airflow so that the heat transfer through convection is reduced. Besides, thermal resistance to air (by assuming natural convection) is much larger than



(a) (b)

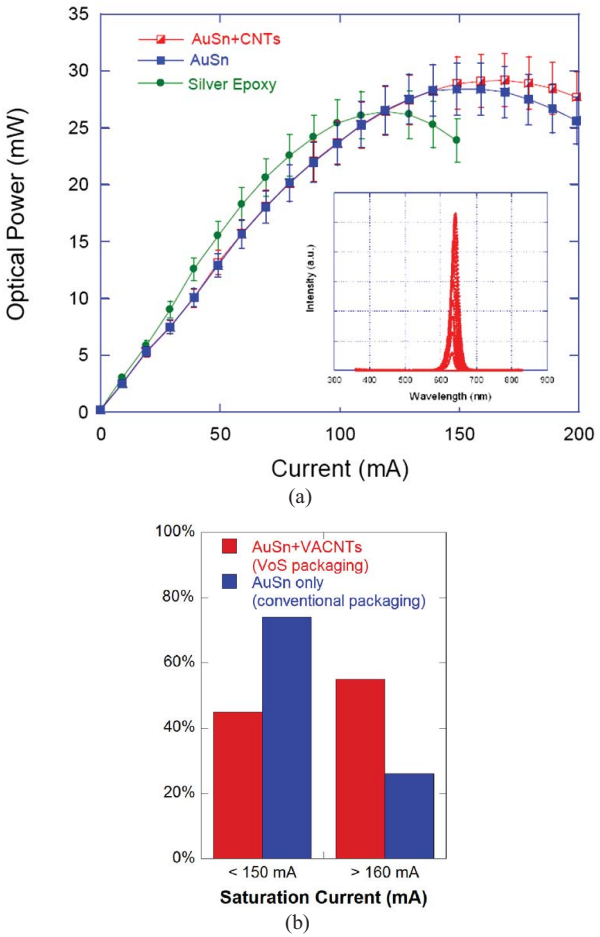
Fig. 6. (a) Schematic diagram and (b) photograph of the packaged LED module.

TABLE II
MEASURED TEMPERATURES AND THERMAL RESISTANCES

Package platform	Heat rate (W)	T_j (°C)	T_{SMD} (°C)	$R_{th(Meas.)}$ (K/W)	$R_{th(Cal.)}$ (K/W)
VoS	0.765	55.5	30.8	**32.3**	**24.5**
Silicon+Au-Sn	0.785	58.5	30.7	**35.4**	**28.1**
Silicon+silver epoxy	0.75	66.7	30.7	**48.0**	**38.8**

that through the substrate. The measured temperatures and the corresponding thermal resistances are summarized in Table II. The thermal resistance of the whole LED module is measured to be 48.0 and 35.4 K/W for the packaging on planar silicon submounts with silver epoxy and Au–Sn solder, respectively. In contrast, the thermal resistance of the LED module packaged on the VoS platform has a thermal resistance of 32.3 K/W. The reduced thermal resistance for the VoS platform indicates that the VACNTs provide both good thermal contact and enhanced thermal conduction.

For comparison, the thermal resistance of the packaged LED module, including the LED chip, submount, and the bonding material between the LED and submount, is simulated to be 38.8 and 28.1 K/W for the reference modules bonded with silver epoxy and Au–Sn solder, respectively. The calculated thermal resistance for the LED bonded on the VoS platform is 24.5 K/W, providing that the thermal conductivity of the VACNT is 300 W/mK. The U-grooves used in the experiments have the dimension of 0.54 area ratio and 0.3 depth ratio. The simulated thermal resistance of the LED chip is 14.8 K/W. Therefore, the theoretical value of the thermal resistance for the planar silicon platform and VoS platform is 13.3 (12.9 without Au–Sn) and 9.4 (9.0 without Au–Sn) K/W, respectively. There exists about the same (7–9 K/W) difference between the measured and simulated thermal resistance of the whole module for the three types of packaged modules. We attribute the difference to the thermal resistance of the bonding materials (silver epoxy) between the submount and the SMD leadframe, which is not included in the simulation due to its uncertain thickness. We also accounted the orthotropic property of bulk thermal conductivity for VACNTs in our simulation model but only found slightly increased overall thermal resistance (~0.07 K/W) of packaged LEDs. This indicates that the thermal resistance of the VoS



(a) (b)

Fig. 7. (a) L–I–V characteristics of the final packaged LED device and (b) histogram of the saturation current for the LEDs packaged on the VoS platform (Au–Sn+CNT) and on planar silicon substrate with Au–Sn solder.

platform is dominated by the axial heat dissipation of the CNTs. Thus, the effect of the orthotropic property of CNTs is negligible for the overall thermal resistance.

The reduction in the thermal resistance can have significant effects when the VoS platform is applied to package high-brightness LEDs, which have relatively large device areas and consume a large power (>10 W). The large device area allows the use of a larger area ratio to incorporate VACNTs, which will result in a larger reduction in thermal resistance, as can be seen from Fig. 2(a). The reduction in thermal resistance is critical for ensuring long lifetime for the high power operation.

V. Conclusion

The packaging with the VoS platform can benefit the device performance more when the heat source is placed closer to the CNTs. This can usually be performed by using the flip-chip bonding technique. For example, the platform can be used for flip-chip bonding of a high-power edge-emitting laser or laser array such that the heat generated in the active layers can be effectively removed by the CNTs. Another example is the flip-chip packaging of high-power blue LEDs with transparent substrates. The ratio of thermal resistance reduction will be larger than the case demonstrated here since the heat will be conducted directly to the VoS platform without passing through the LED substrate.

In conclusion, we have demonstrated both by simulation and experiments that the VoS platform can provide excellent heat spreading for packaged photonic devices. The simulation indicates that greater than 45% of reduction in the thermal resistance can be achieved by using the VoS platform, by comparing to the use of planar silicon substrate. The application of this platform to packaged LEDs verifies that the VoS platform can provide excellent heat conduction for the LED chips, leading to an increased saturation current and enhanced output power. Thermal resistance of VACNT packaged LEDs is measured to be 32.3 K/W, lower than the values for the modules packaged with the planar silicon substrates. The thermal resistance of the VoS platform can be further reduced by optimizing the platform geometry to increase the volume ratio of VACNTs and improve the thermal conductivity of VACNT.

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